

Figure 1

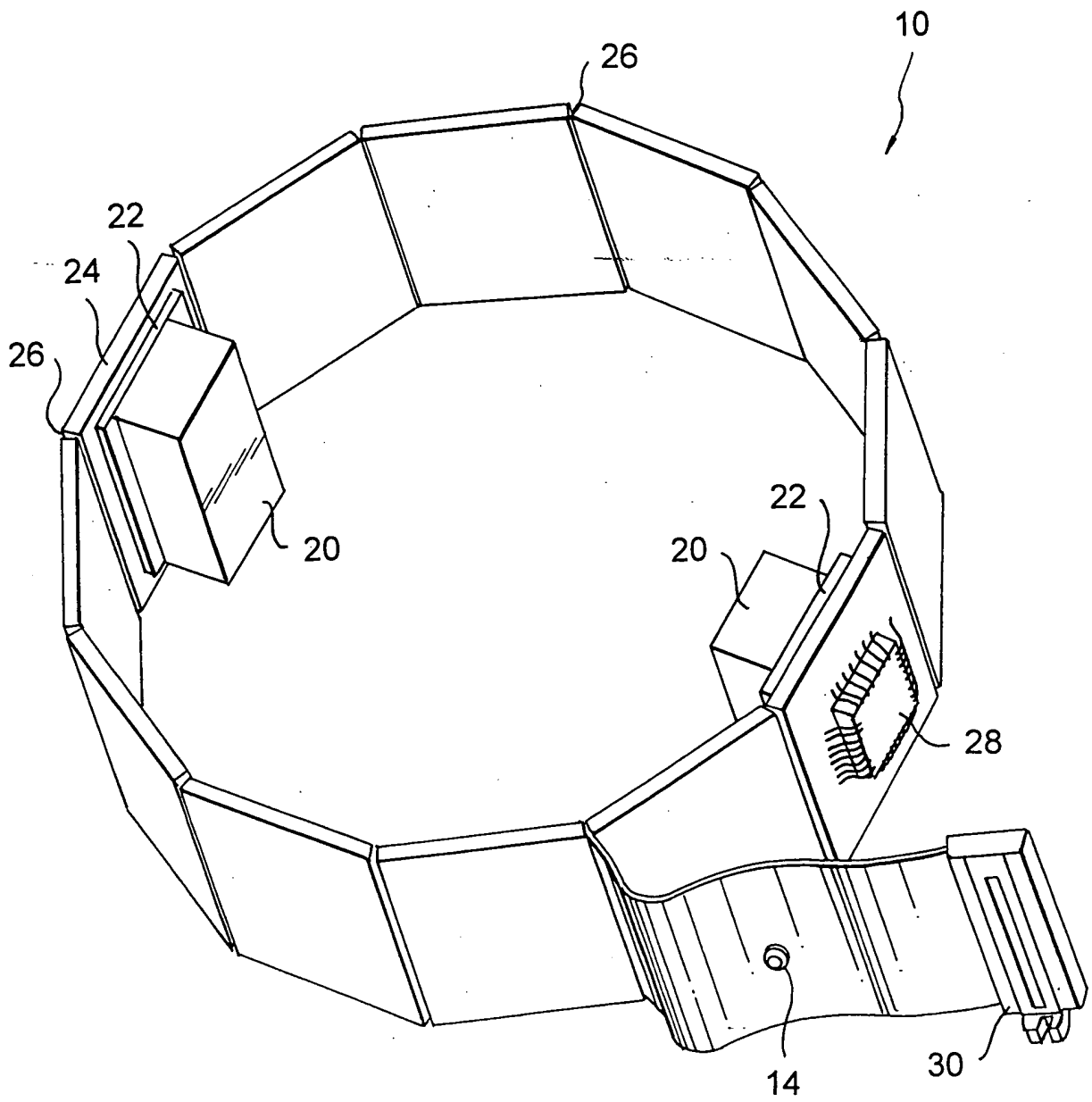


Figure 2a

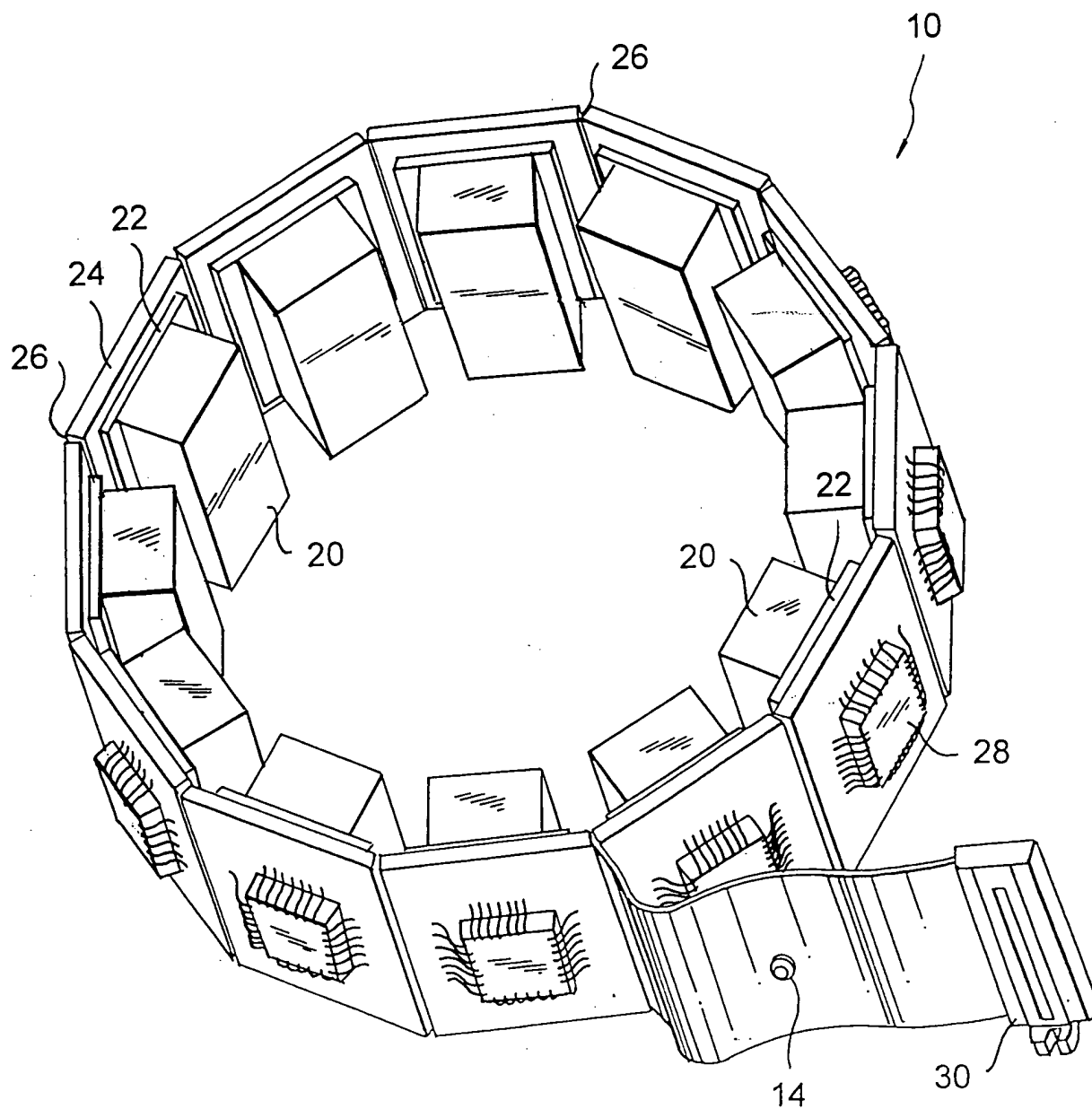


Figure 2b

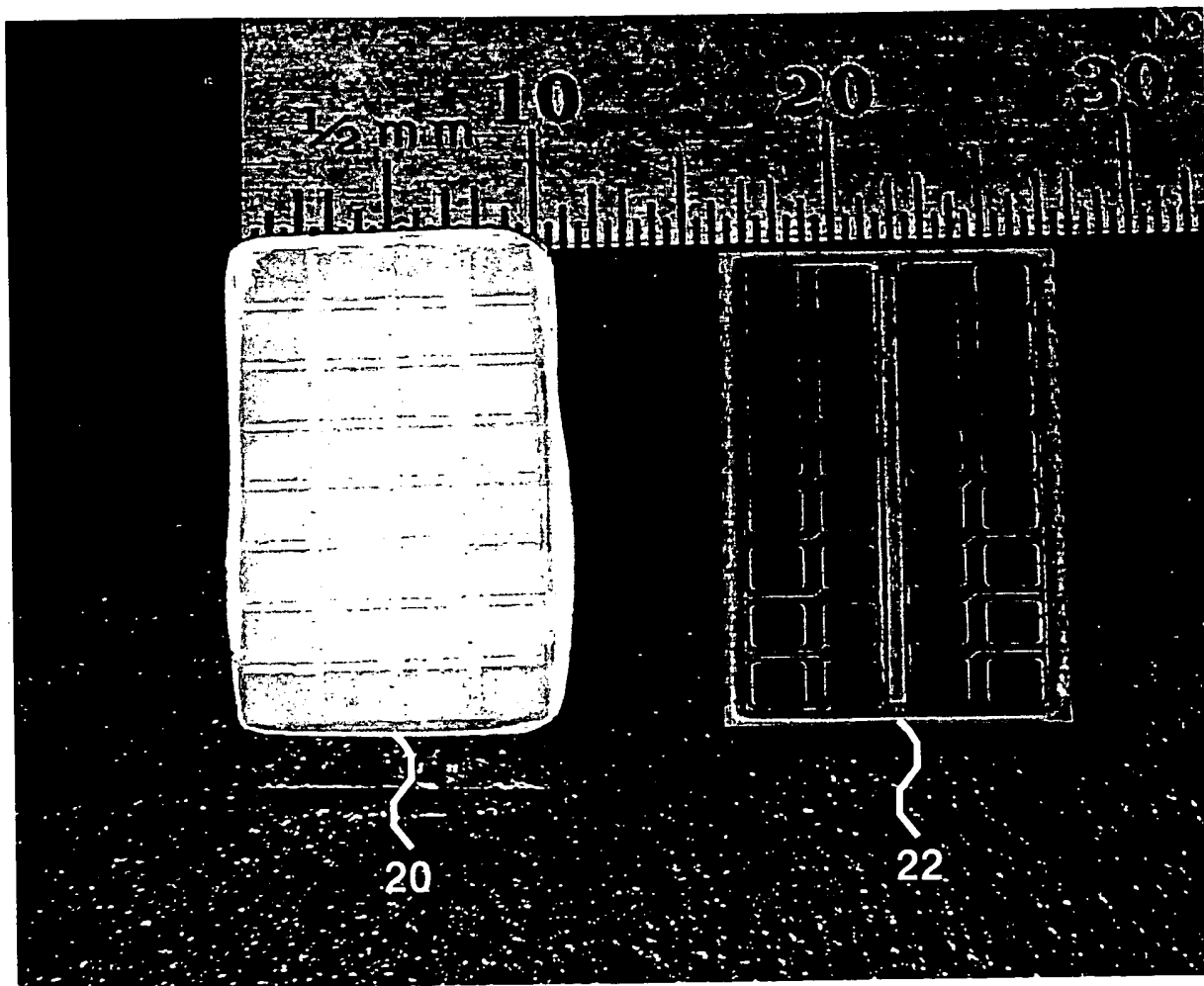


Figure 3

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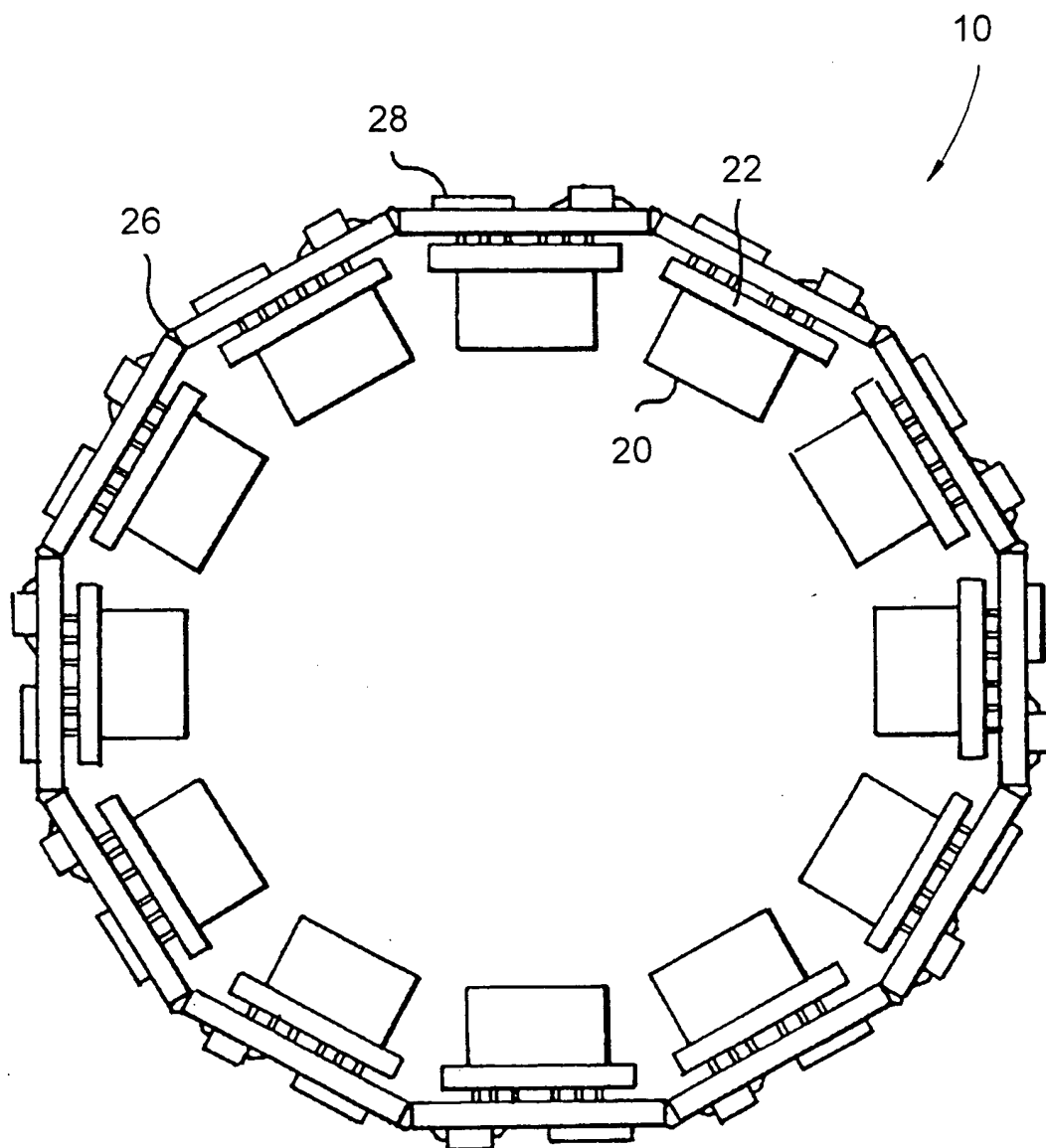
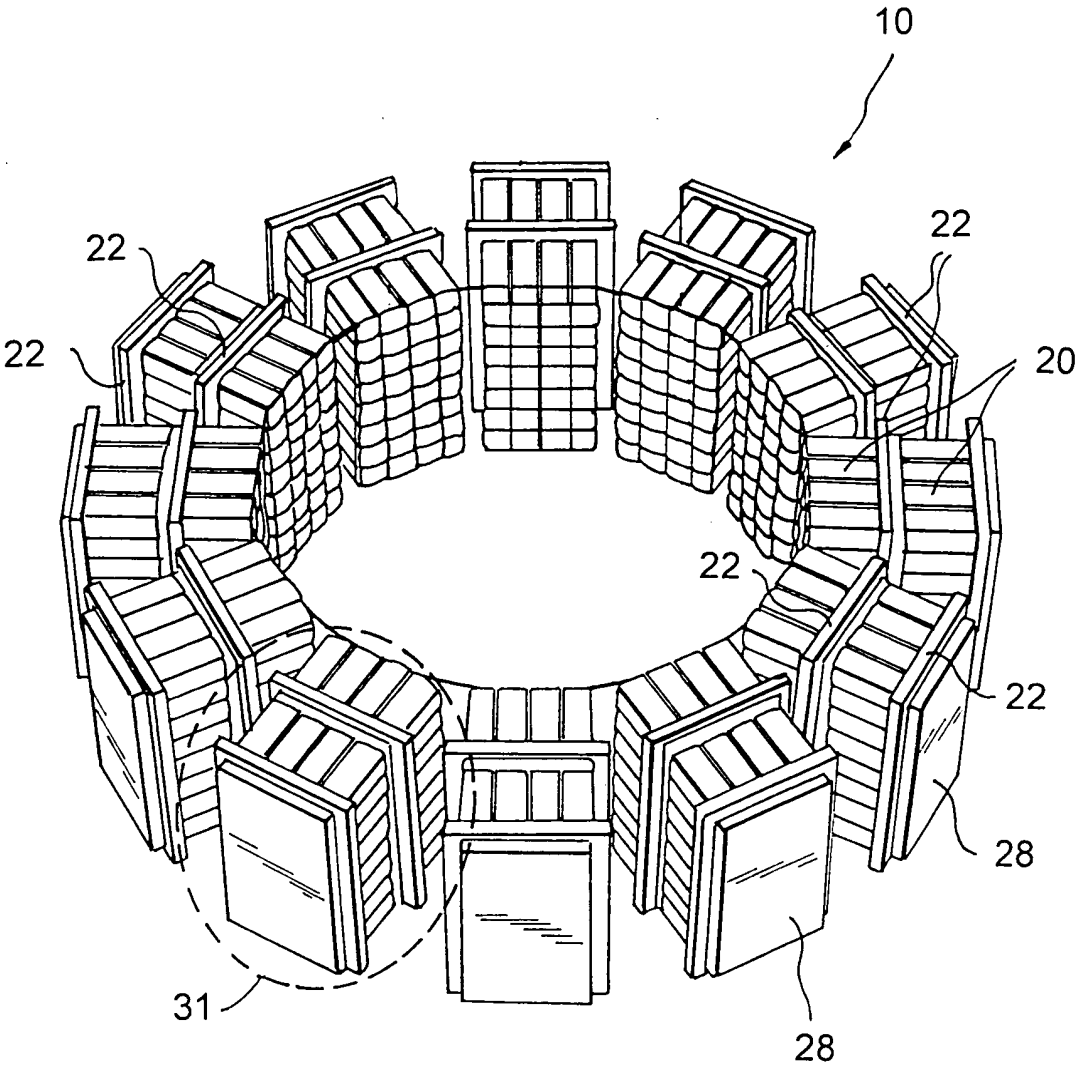
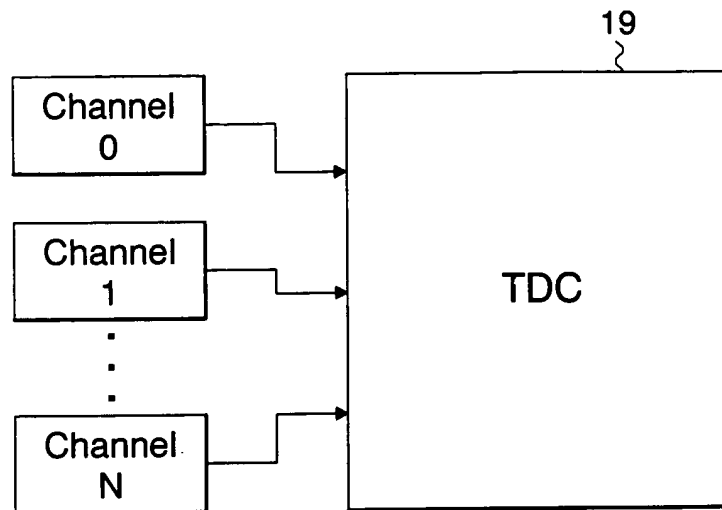


Figure 4

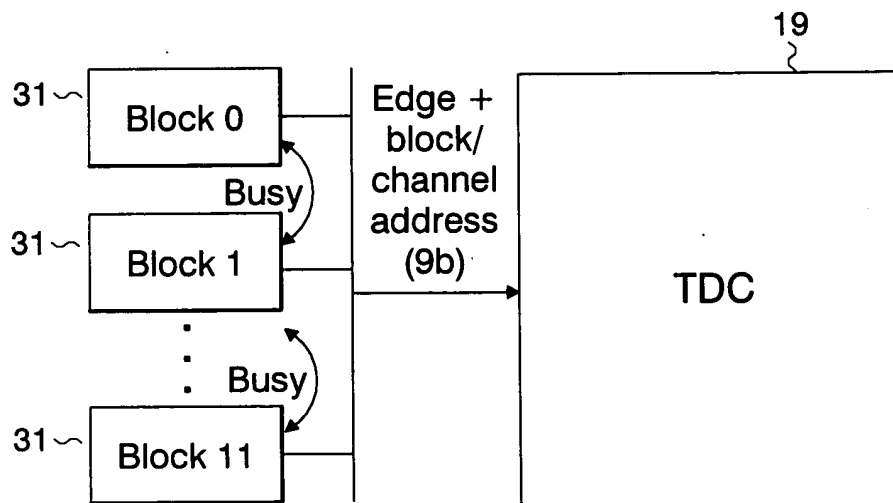
Figure 5





Individual Serial Links

Figure 6
(Prior Art)



Common Serial Bus with Busy

Figure 7

Serial Link Timing

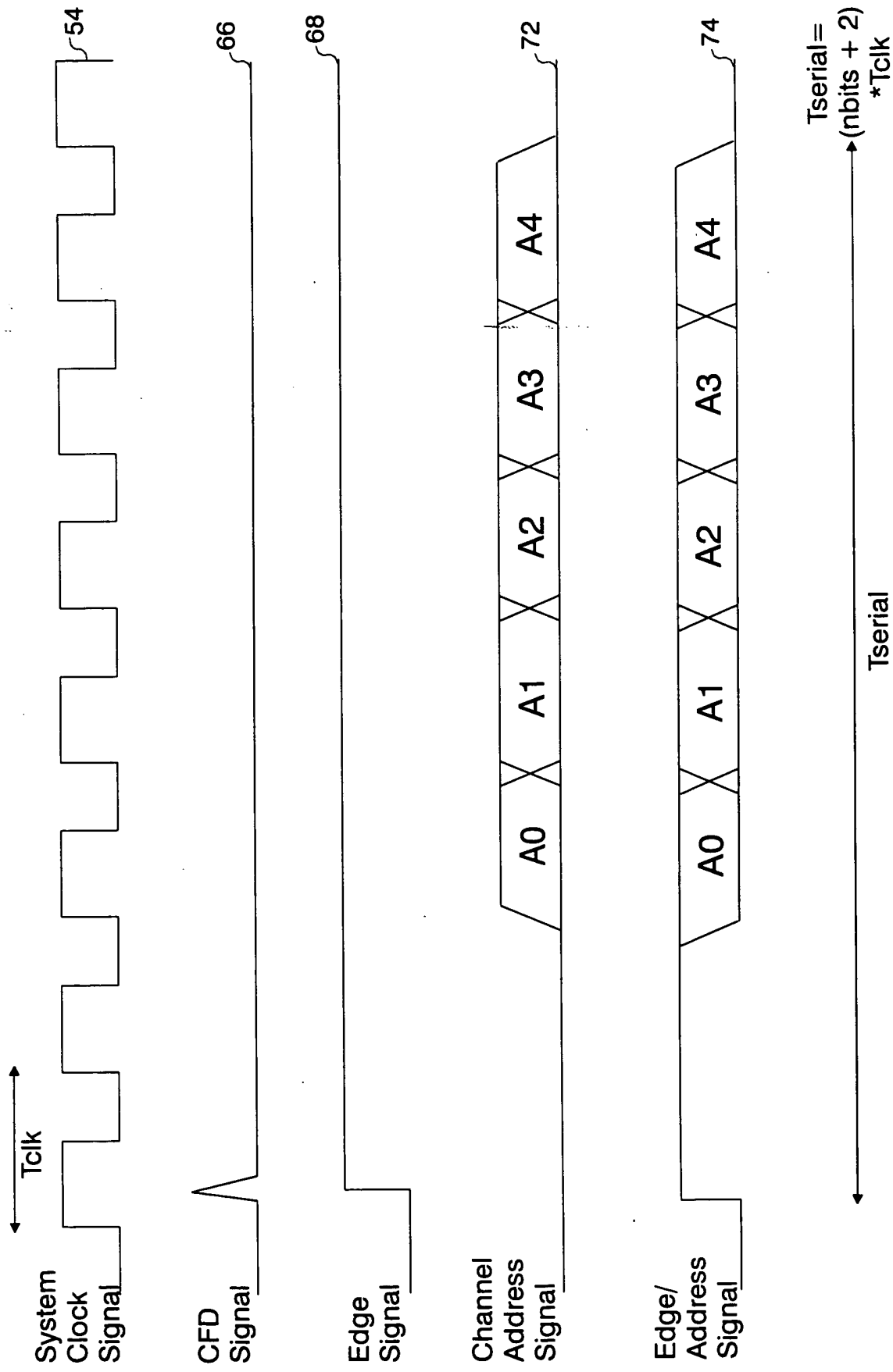


Figure 8

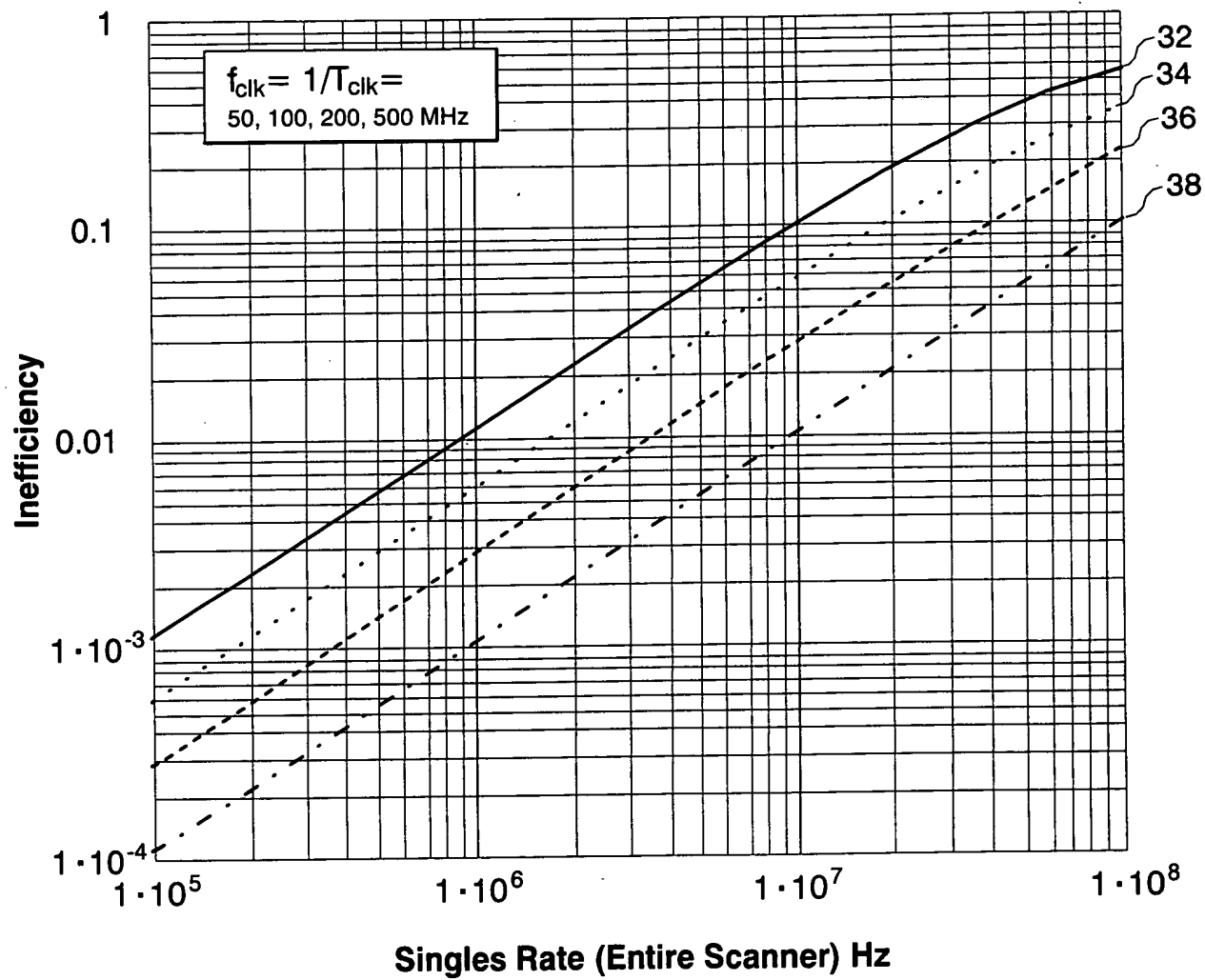


Figure 9

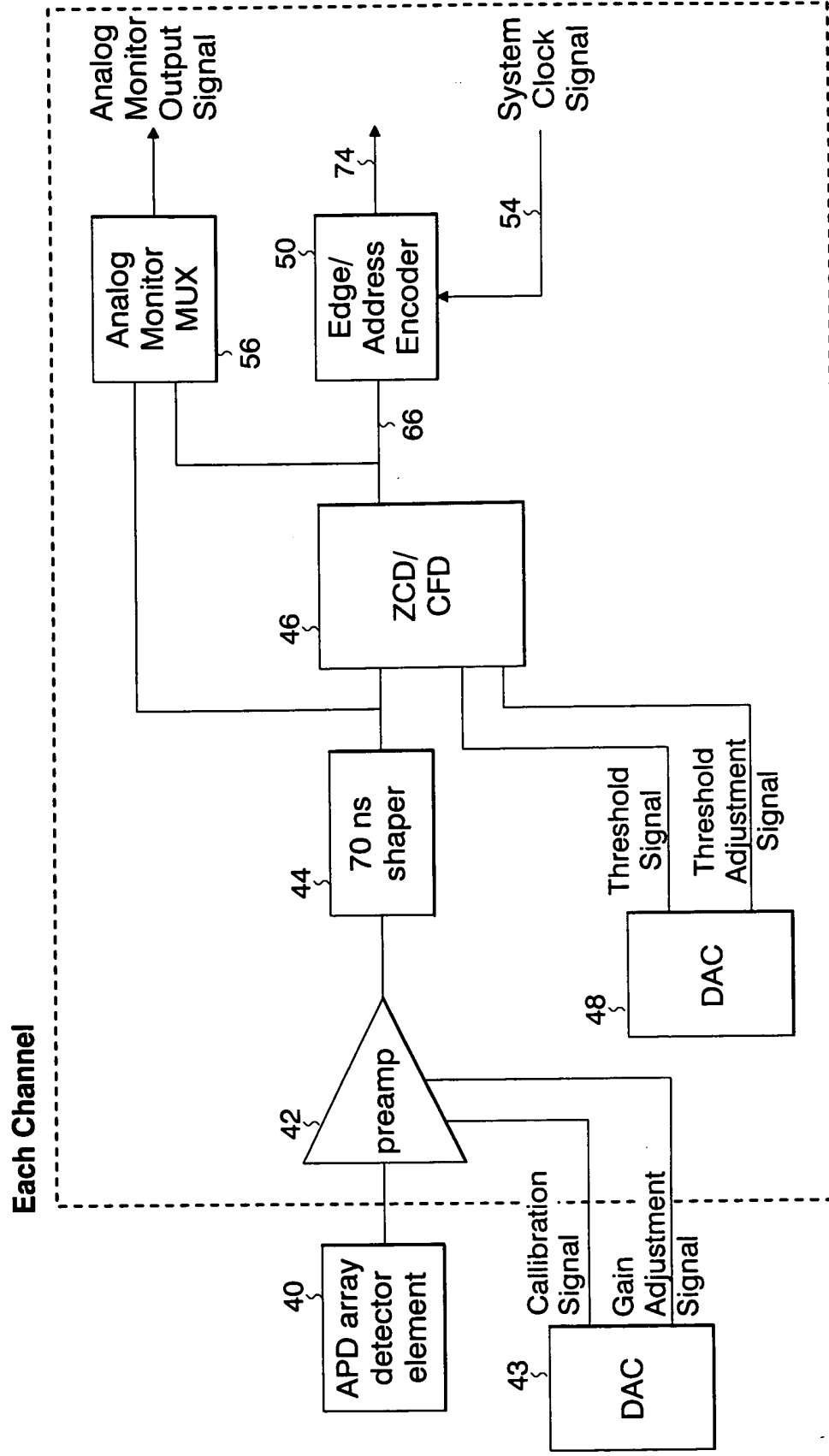


Figure 10

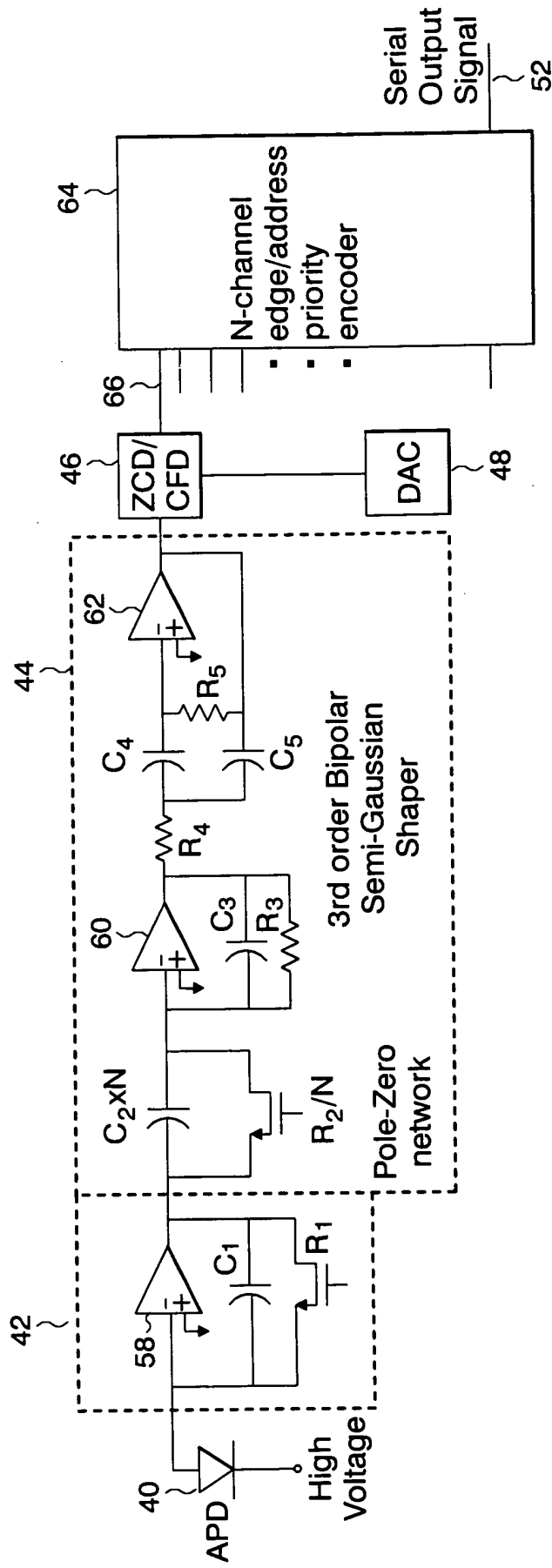


Figure 11

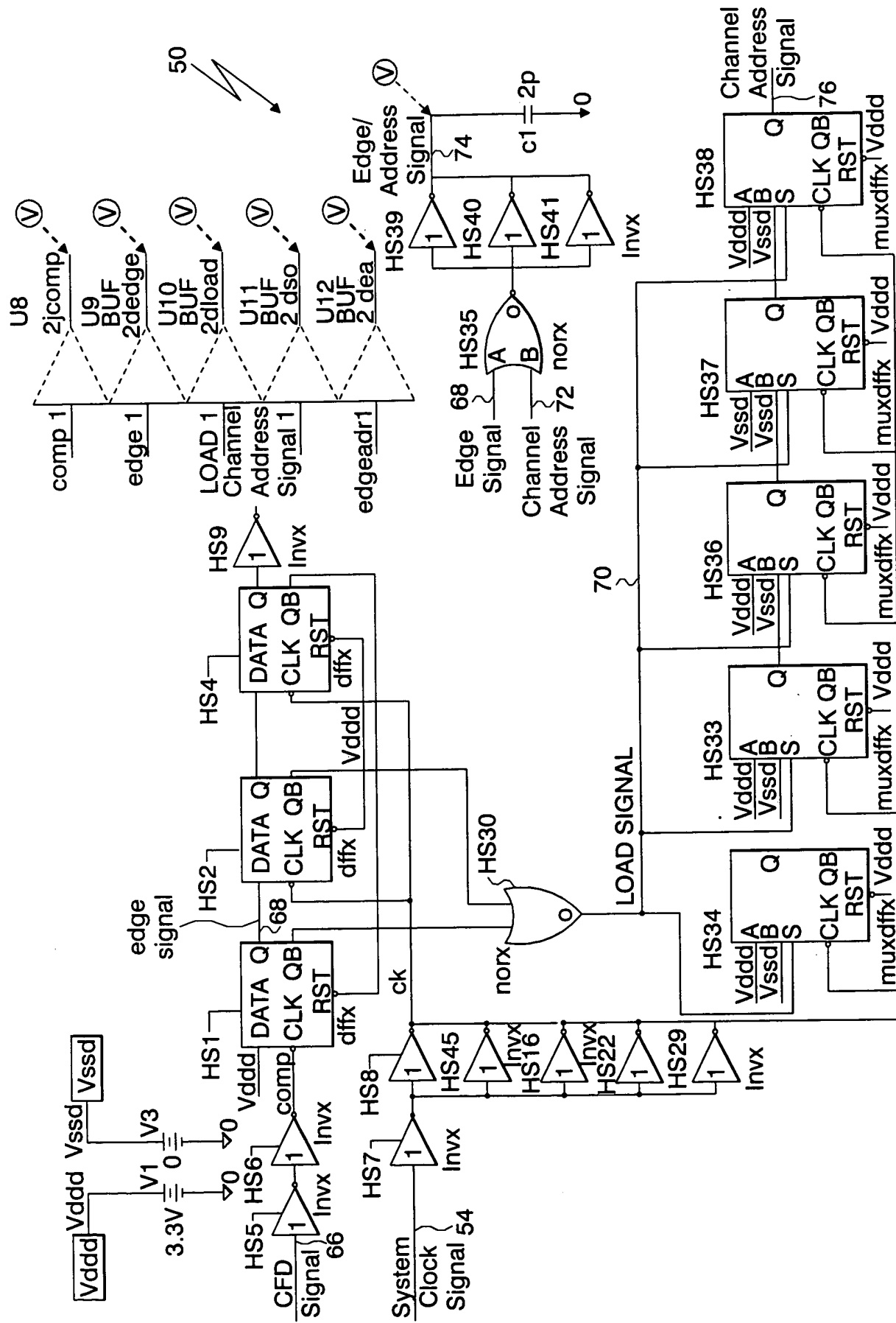


Figure 12

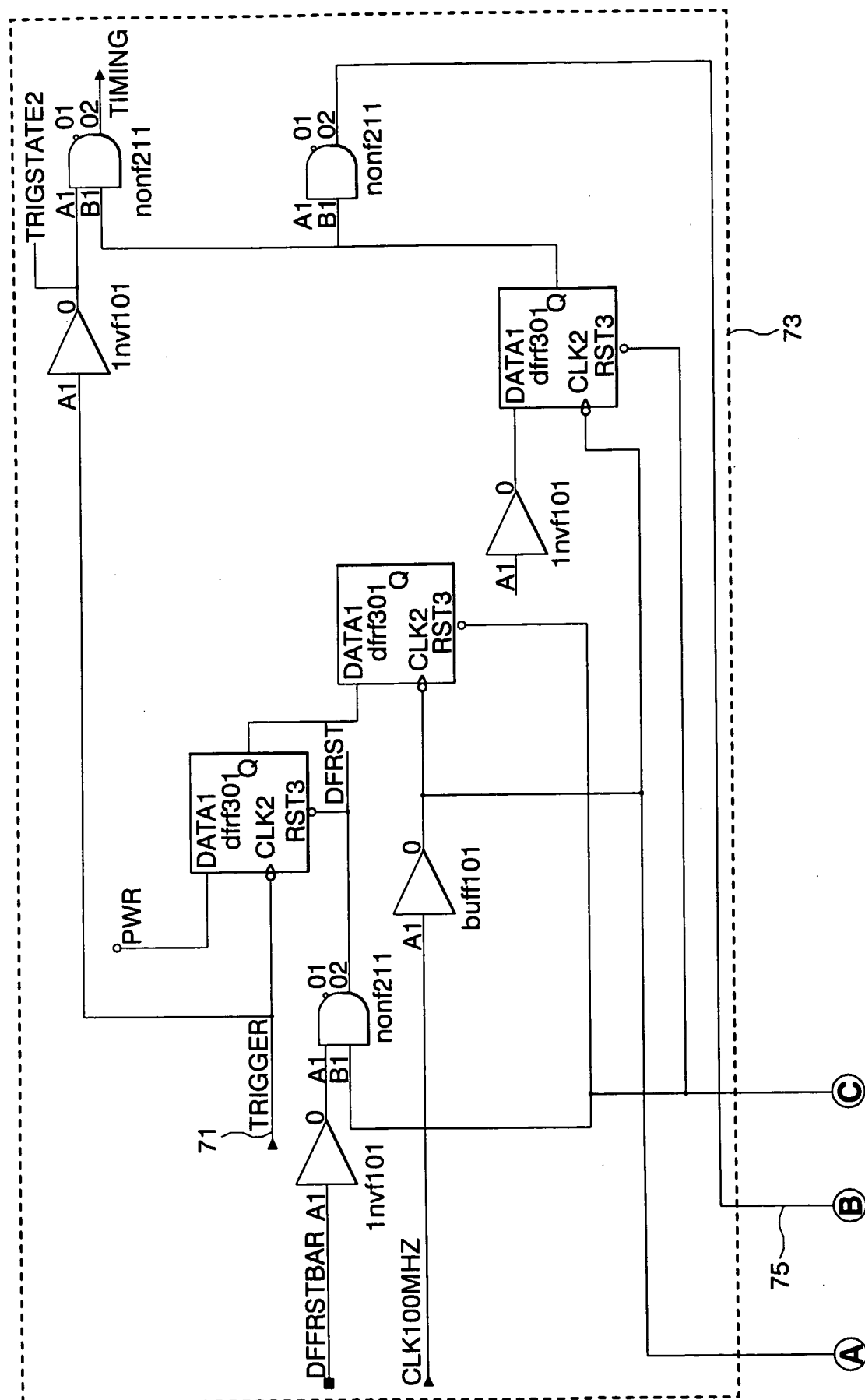
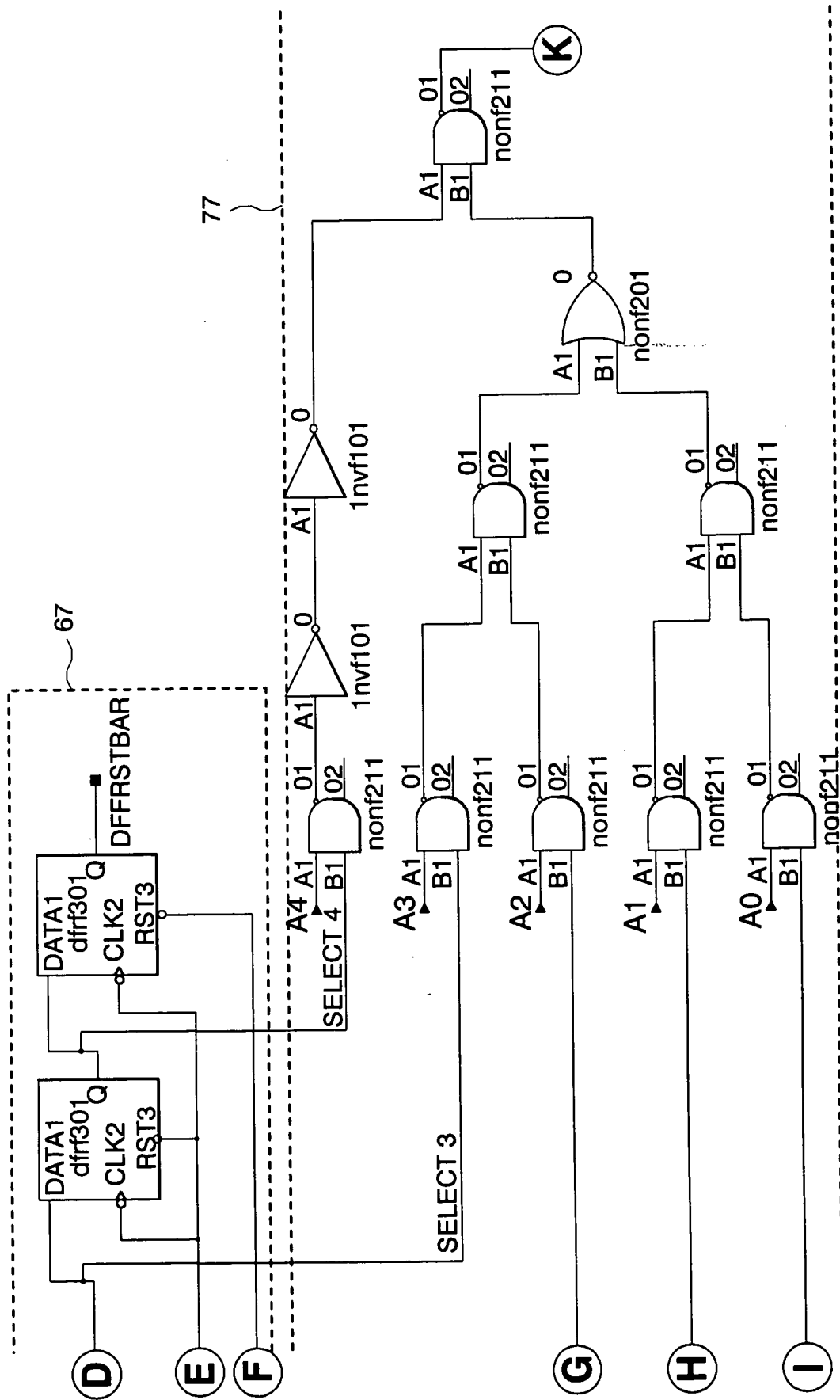


Figure 12a(1)



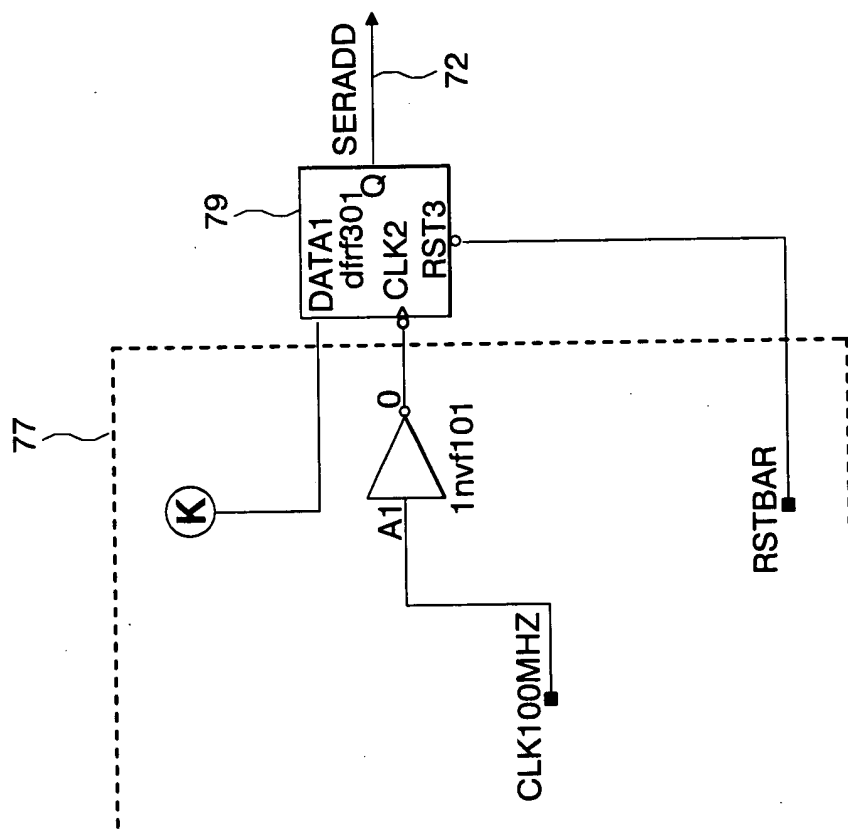


Figure 12a(4)

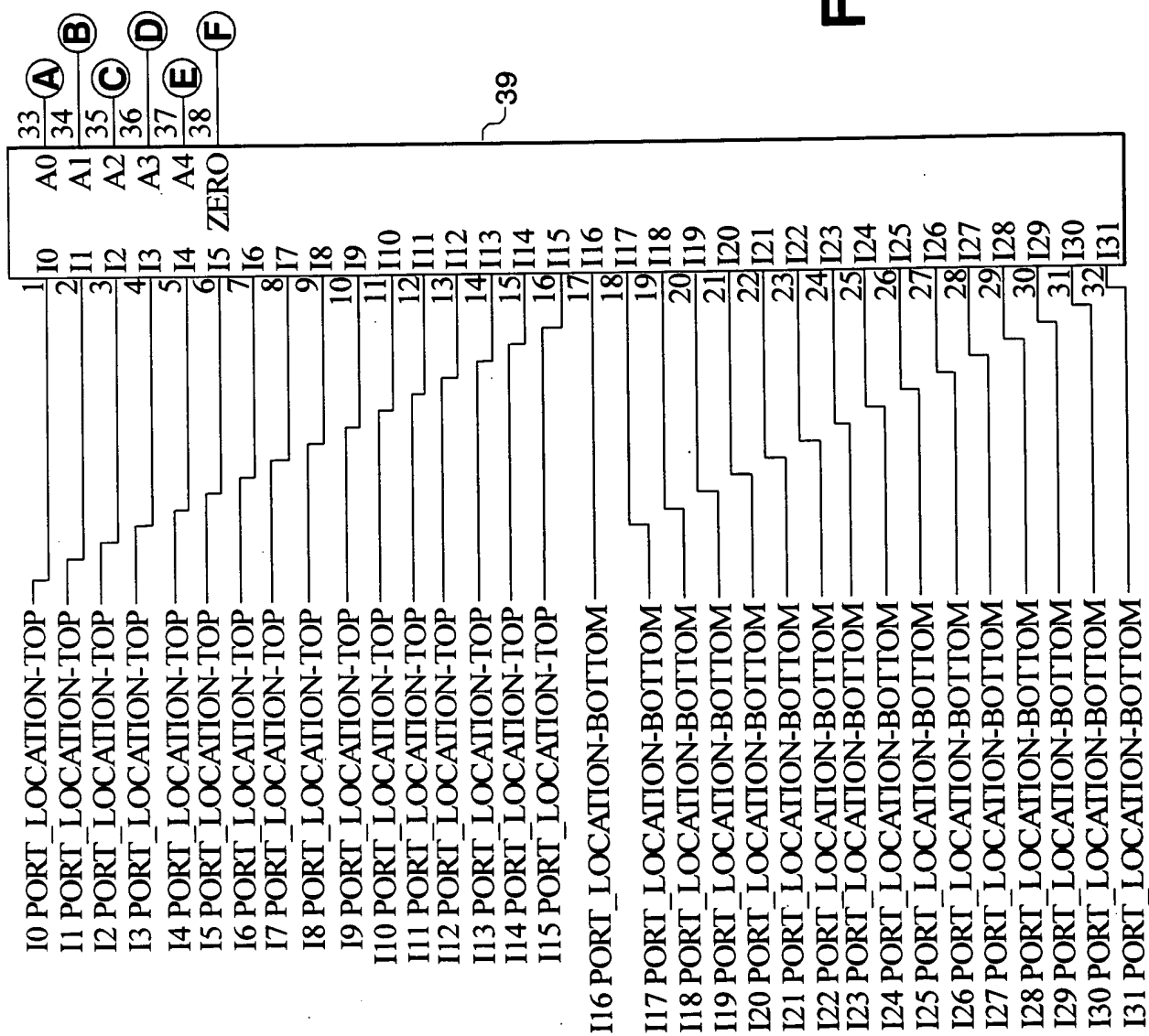


Figure 13(a)

Figure 13(b)

The diagram illustrates the internal logic of the PORT_LOCATION-80 component. It consists of two main logic blocks: a 4-to-1 multiplexer (MUX) and a 4-to-1 MUX. The top MUX has inputs labeled A0, A1, A2, and A3, and outputs labeled CHAND, SEL0, SEL1, SEL2, SEL3, and SEL4. The bottom MUX has inputs labeled SELECT 0, SELECT 1, SELECT 2, SELECT 3, and SELECT 4, and outputs labeled TRIGGER, RSTBAR, CLK, DFFRST, and TRIGSTATE2. The diagram shows how external signals like PORT_LOCATION-BOTTOM, PORT_LOCATION-TRIGGER, and PORT_LOCATION-80 are connected to the internal logic blocks. It also includes a logic gate (A1) that combines signals from the MUX outputs to produce the final output signals: CHAND, PORT_LOCATION-80, and PORT_LOCATION-TRIGGER.

buff101 on this level to be replaced by a cascaded inverter buffer

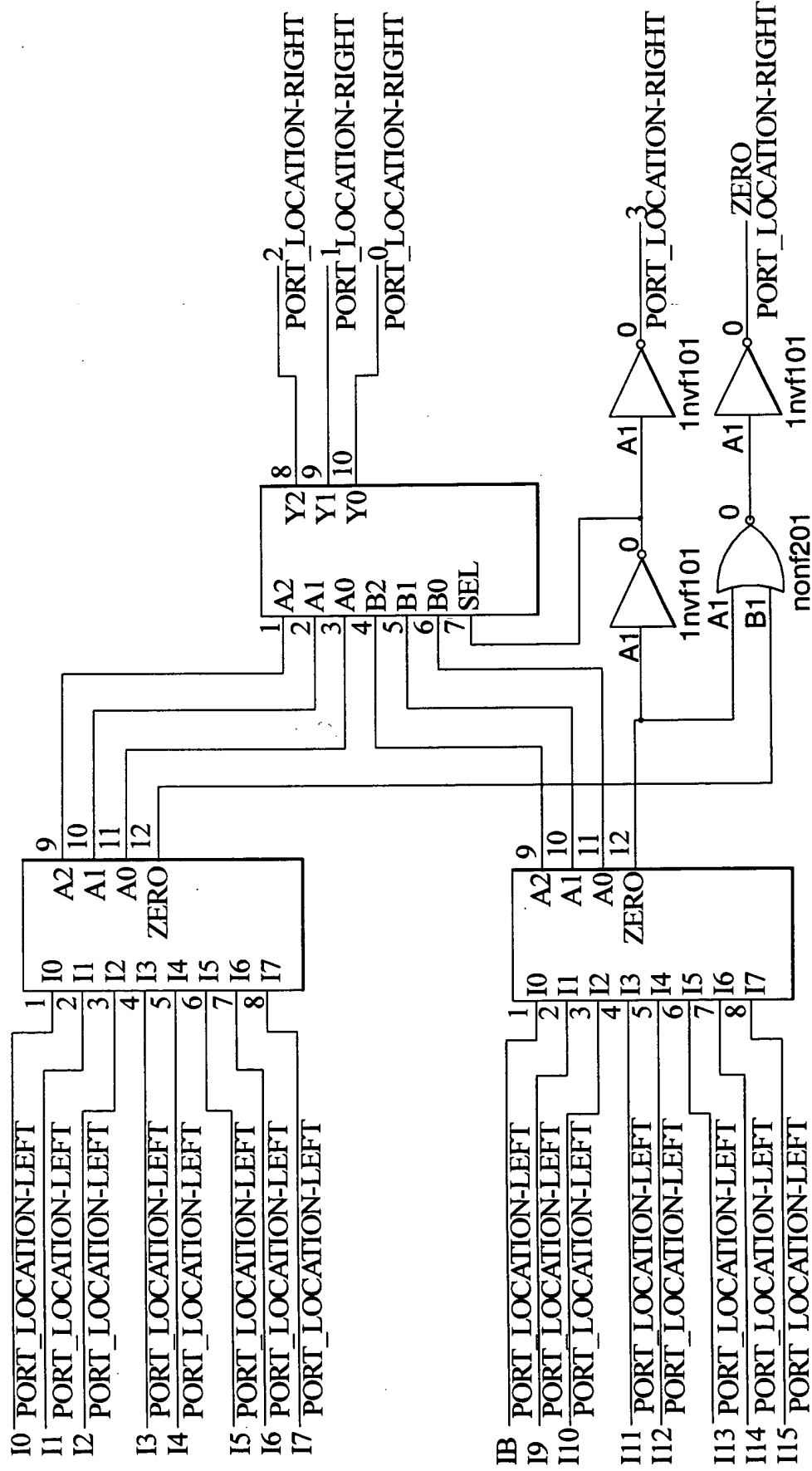


Figure 14

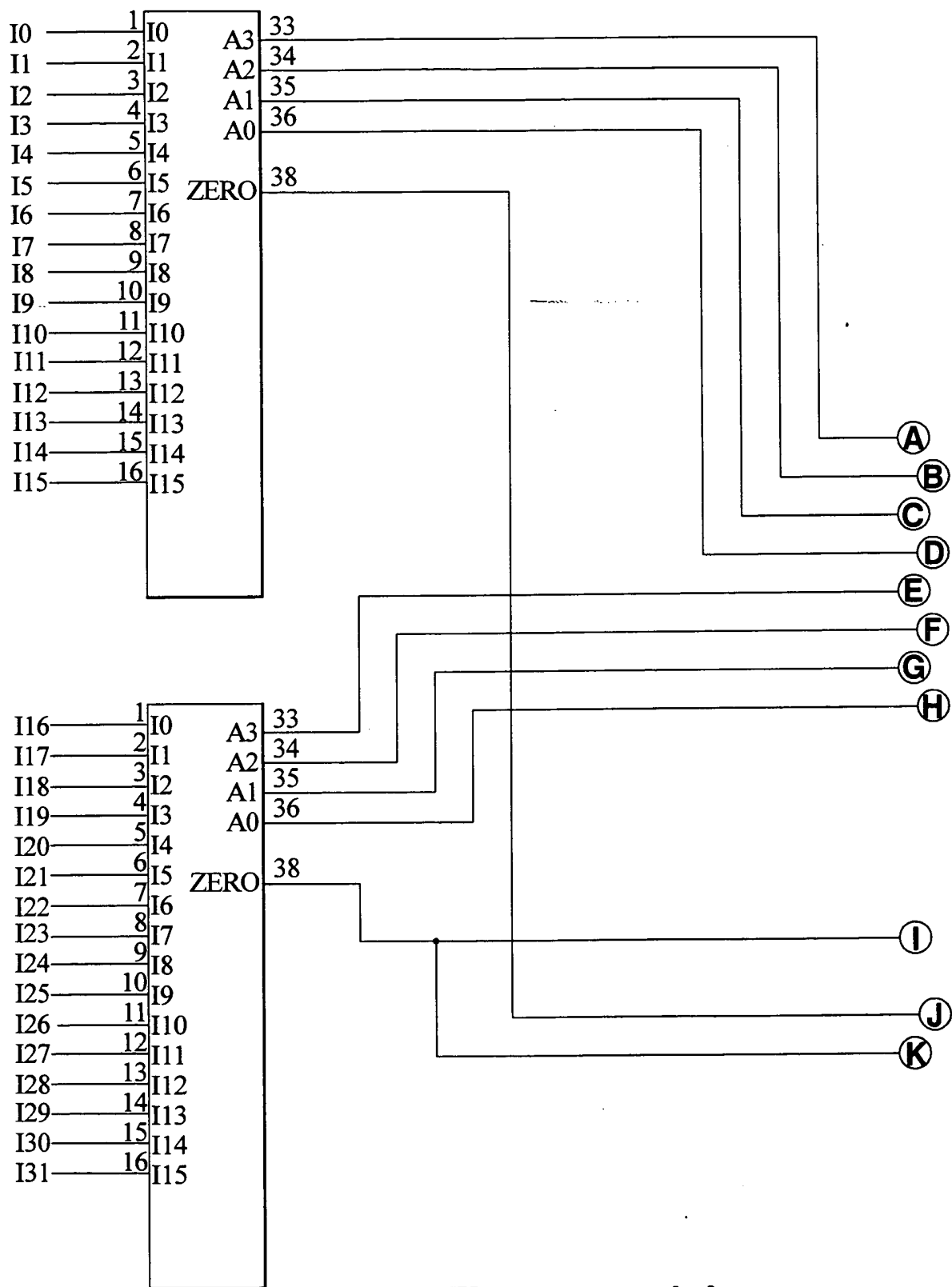


Figure 15(a)

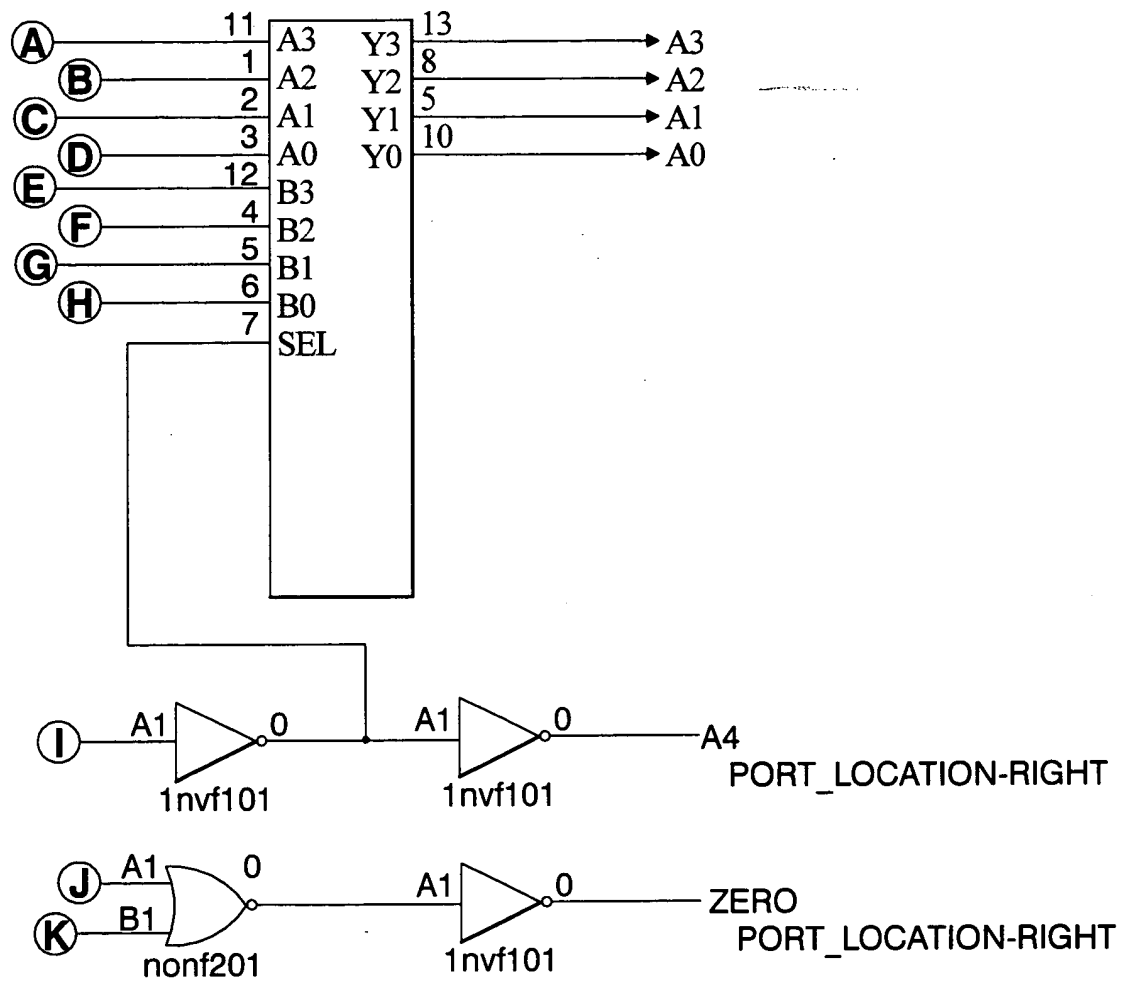


Figure 15(b)

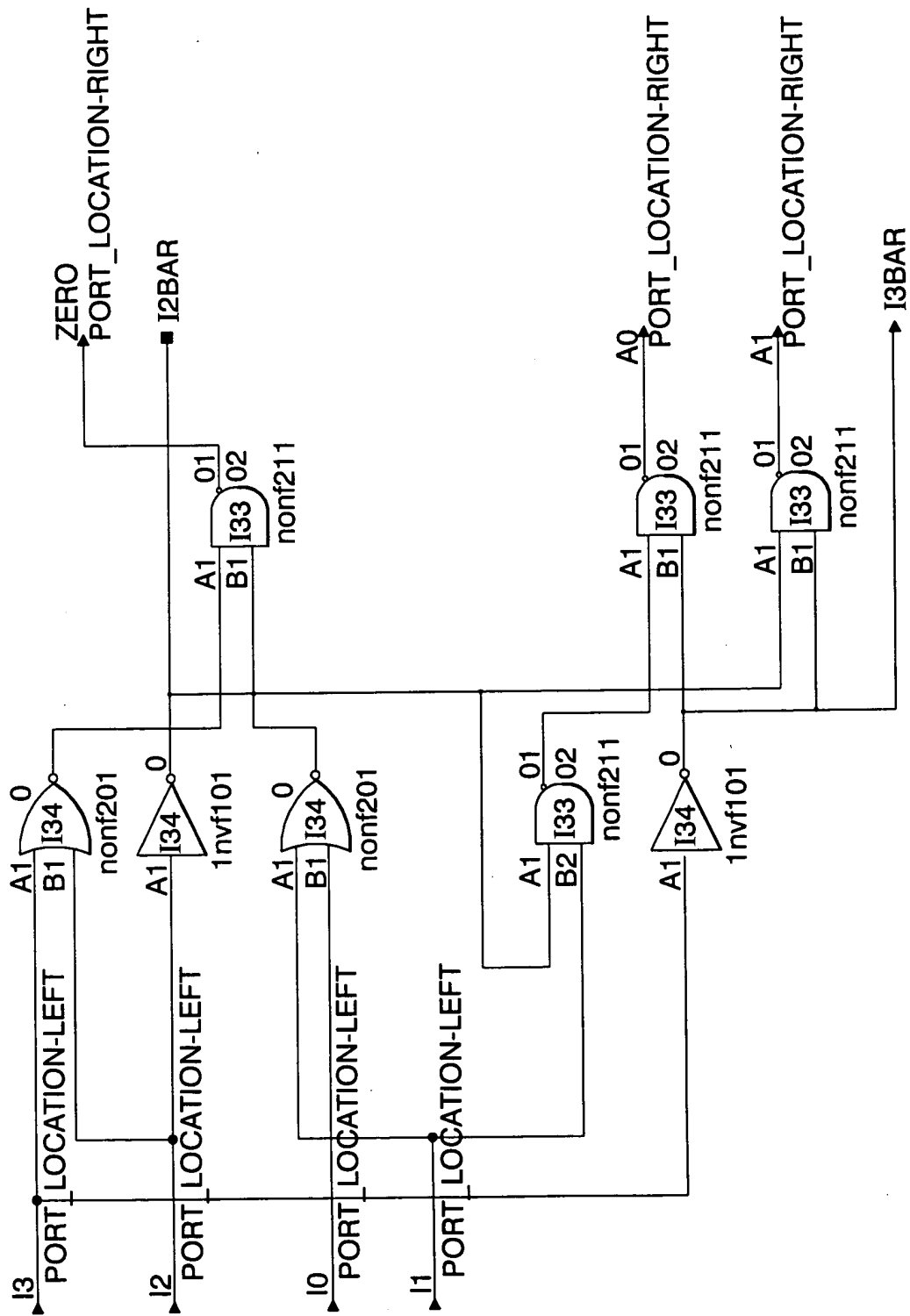


Figure 16

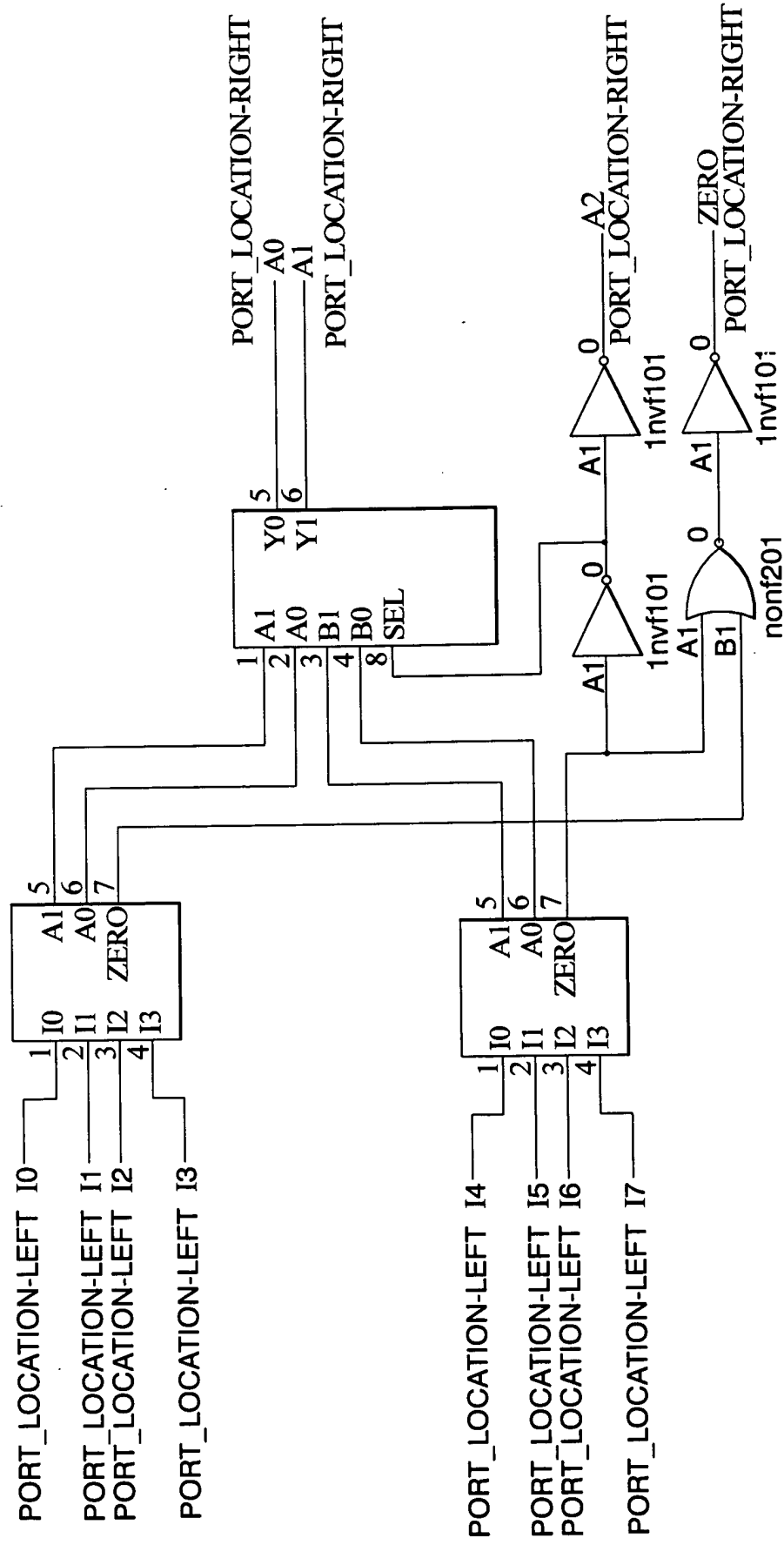


Figure 17

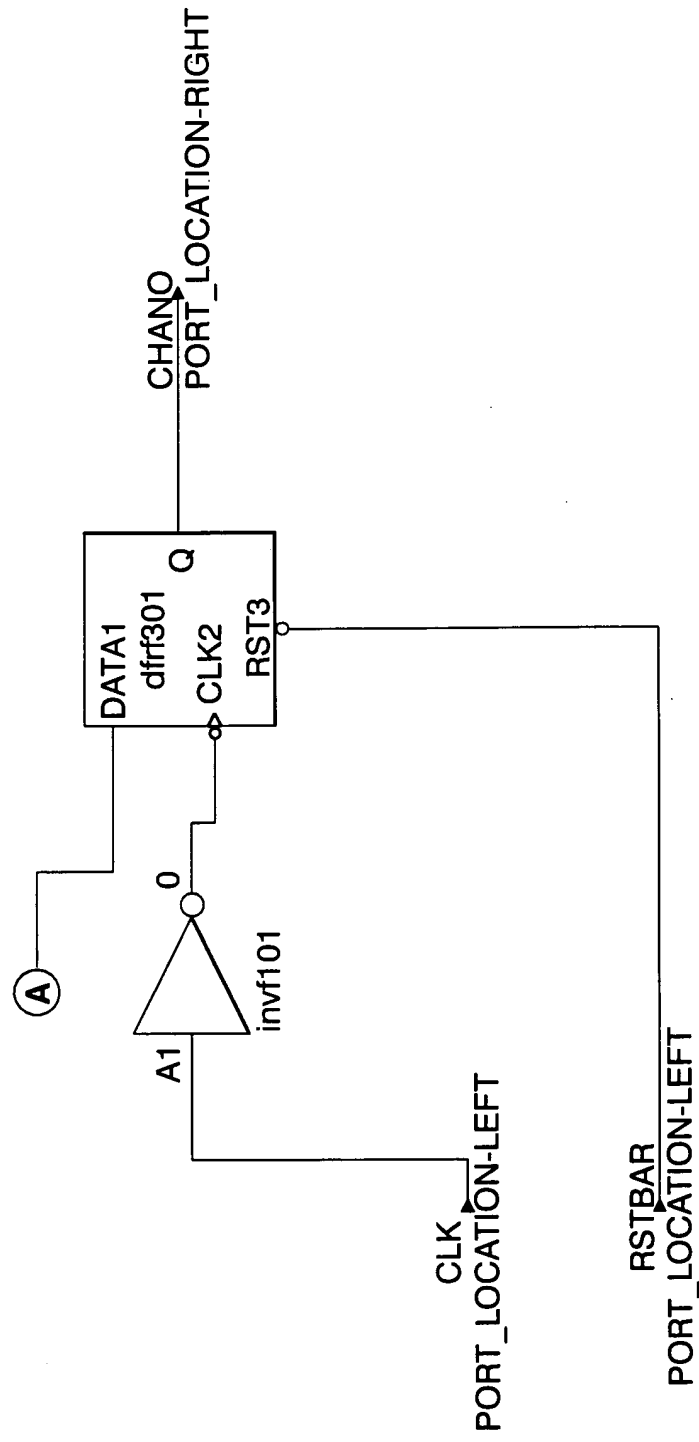


Figure 18(b)

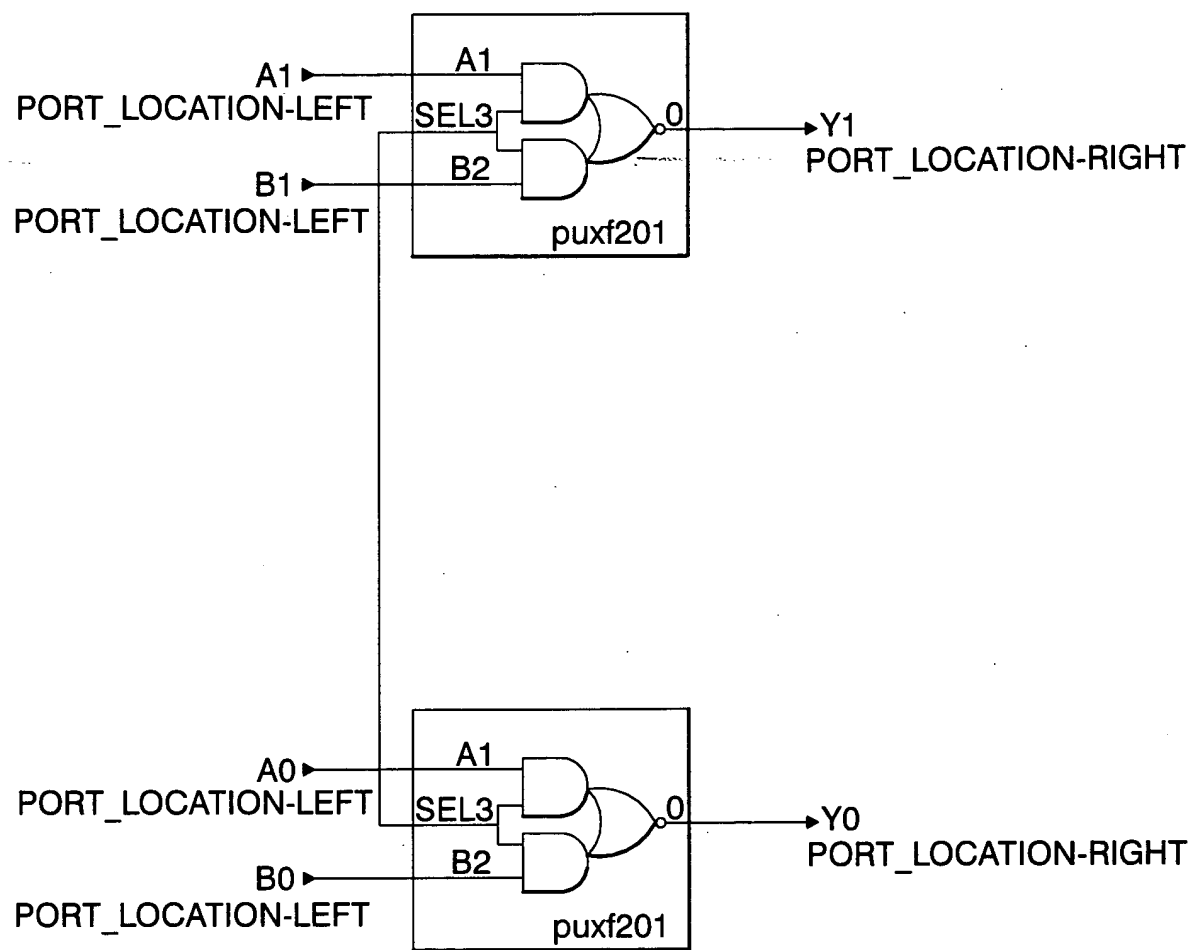


Figure 19

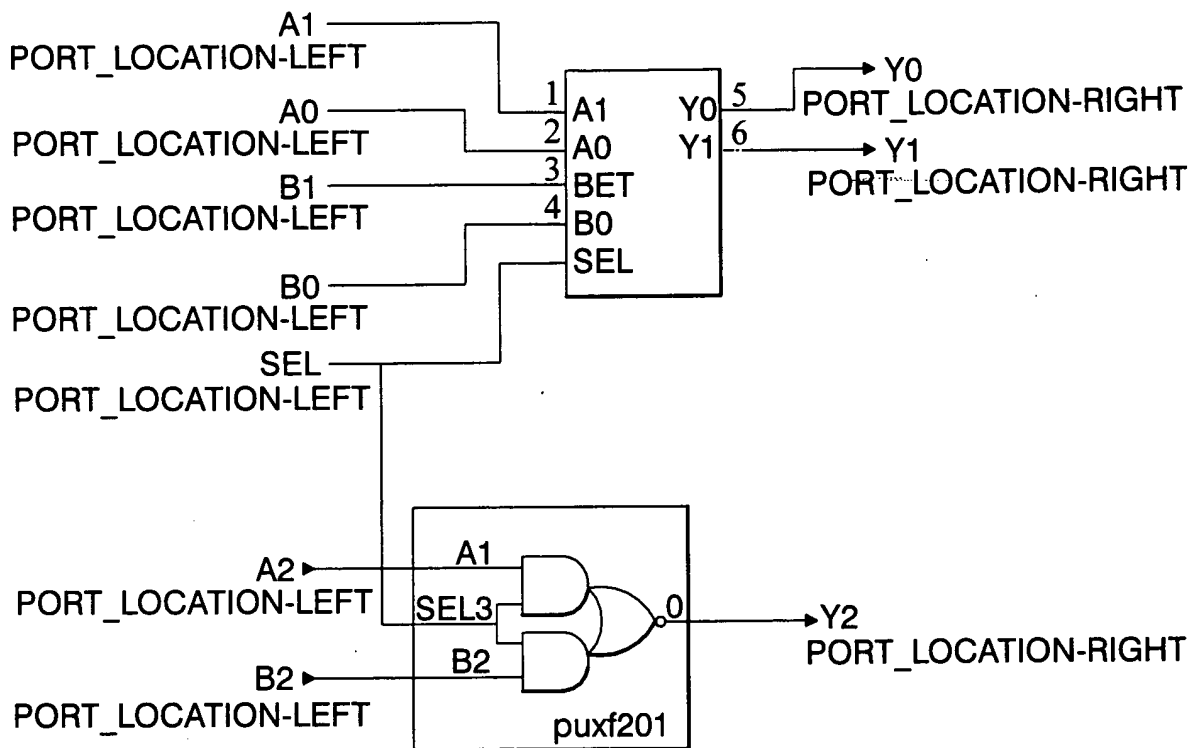


Figure 20

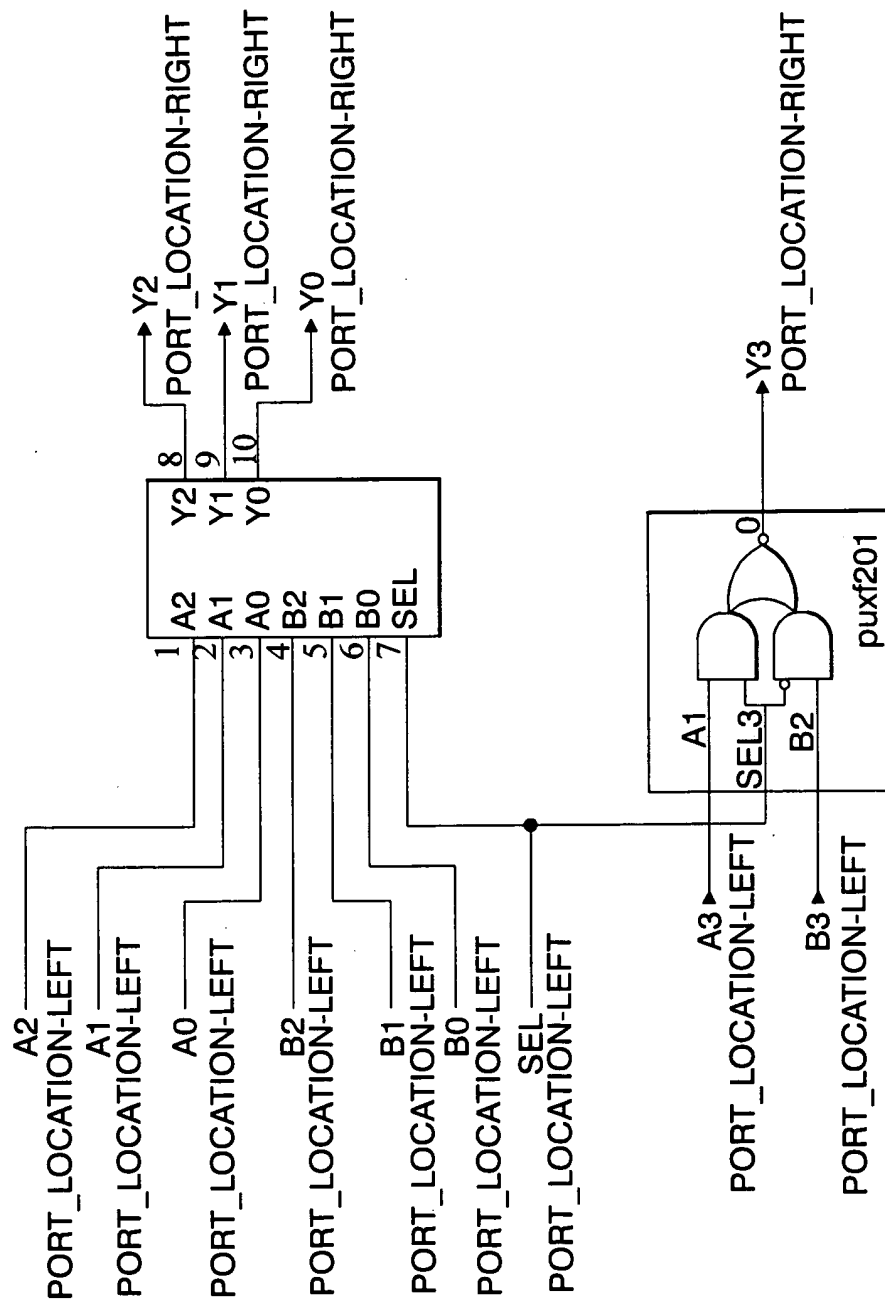


Figure 21



Figure 22(a)

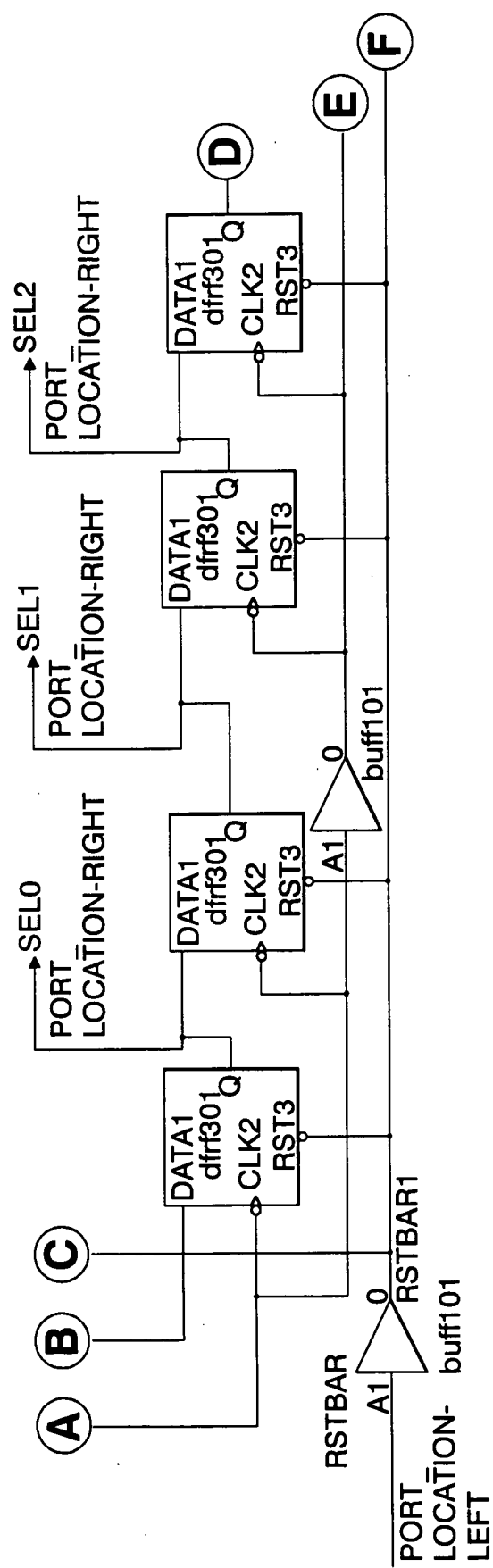


Figure 22(b)

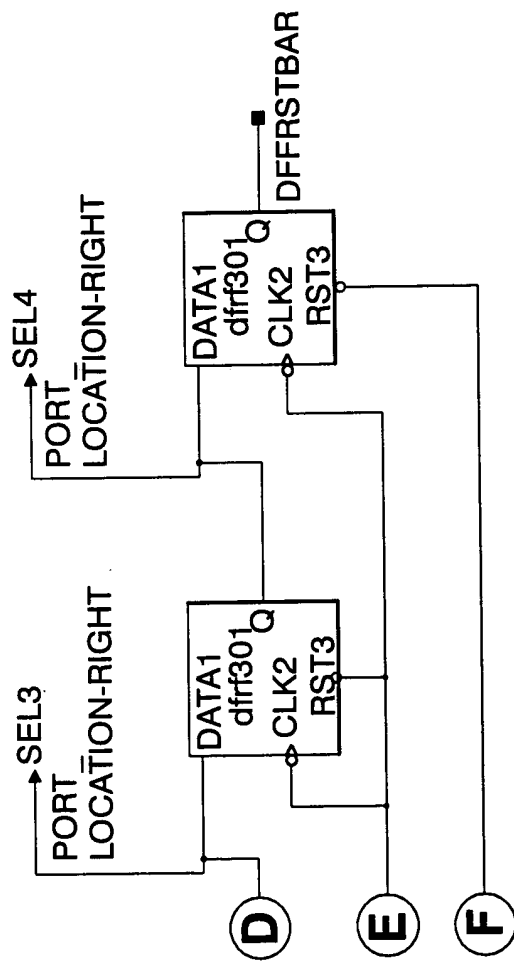


Figure 22(c)

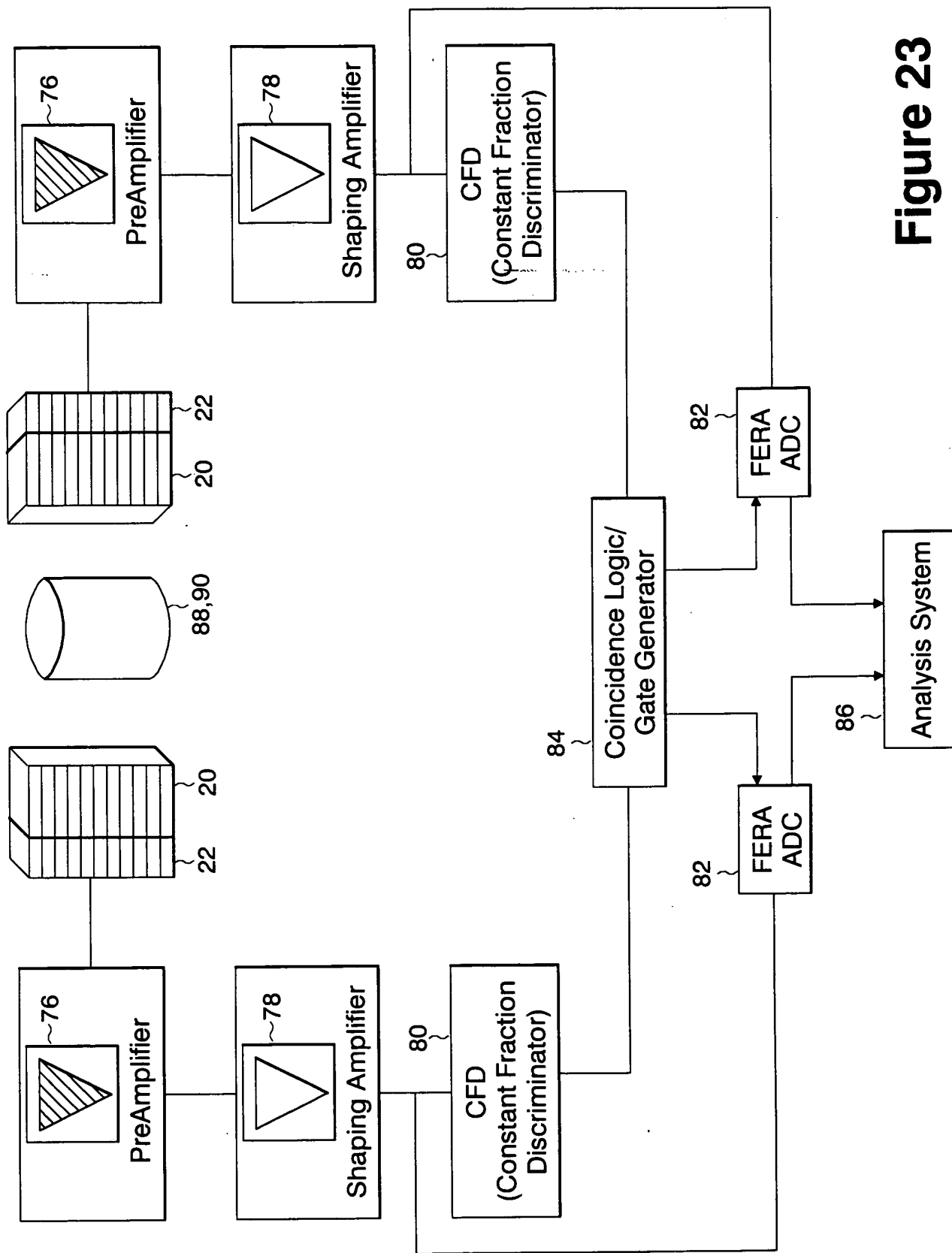


Figure 23

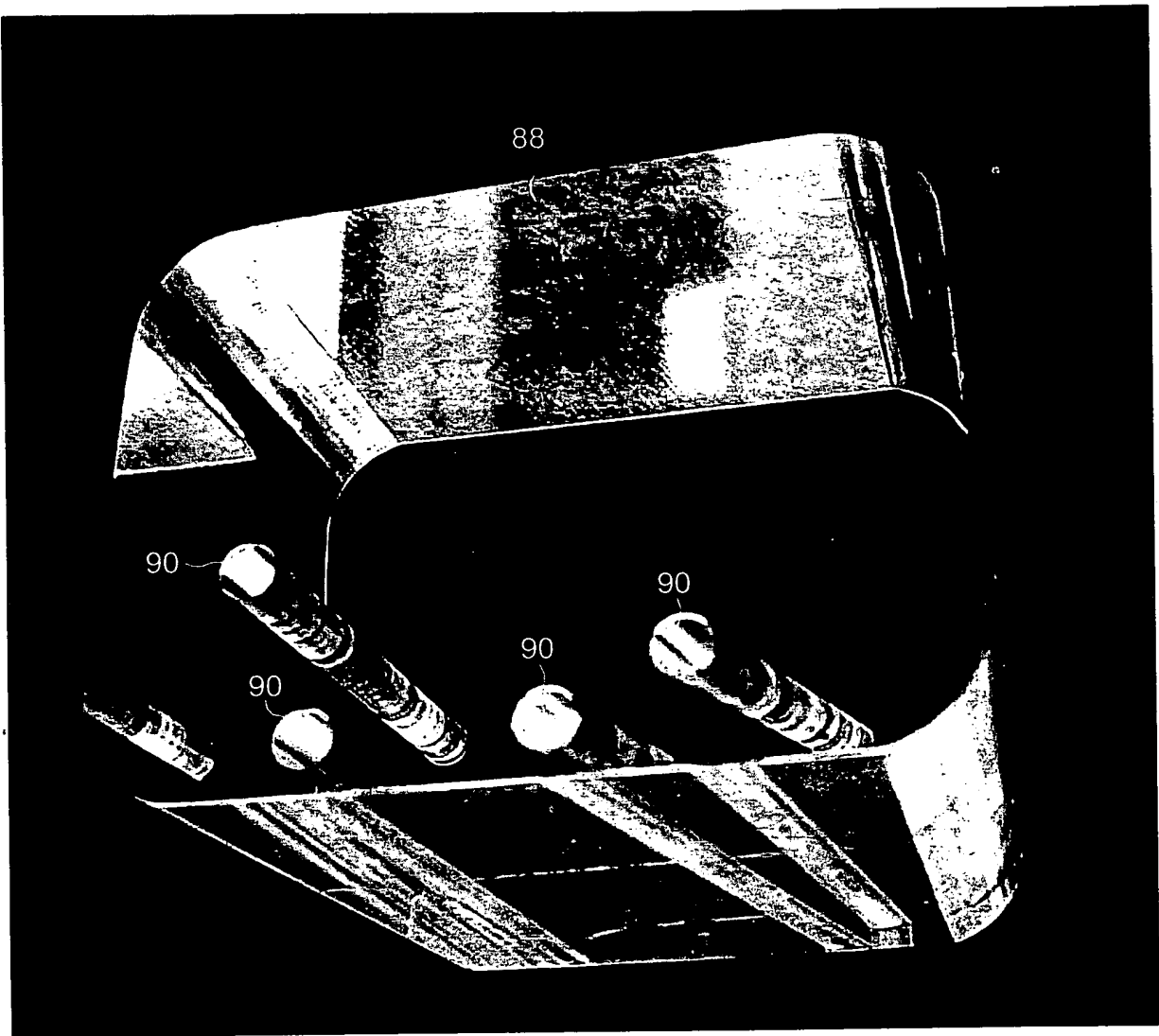
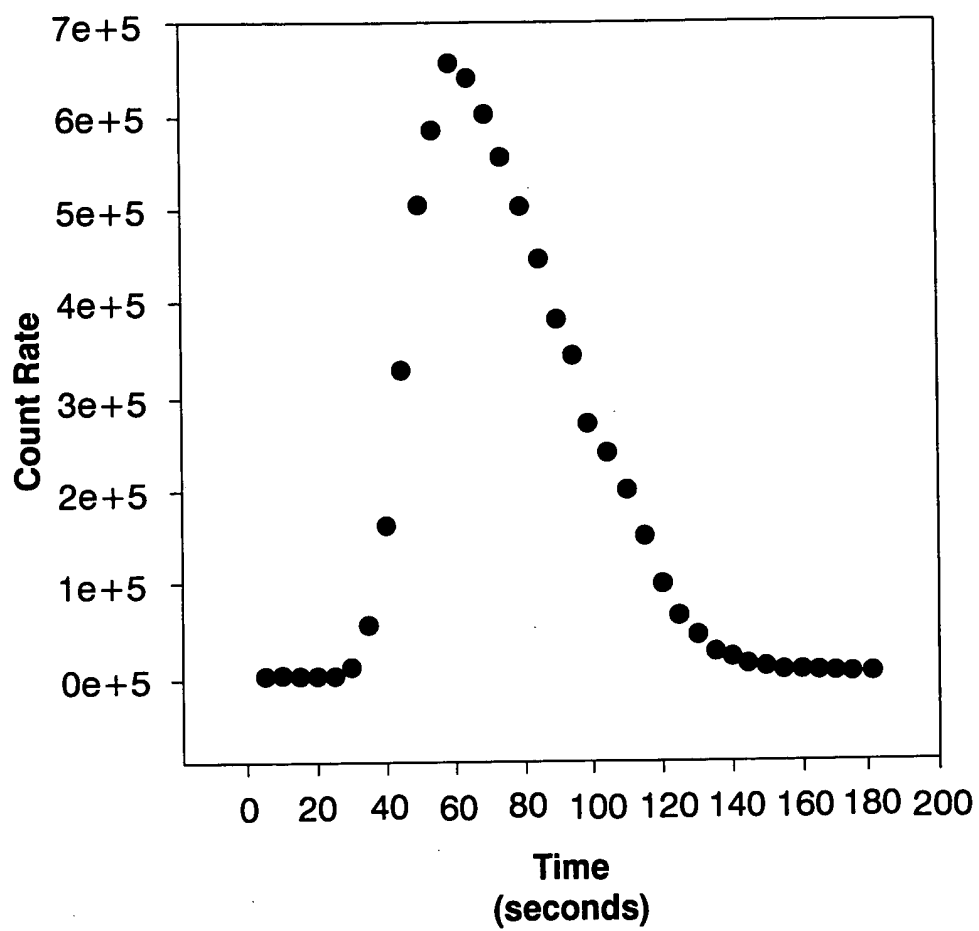


Figure 24

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Input Function

Figure 24a

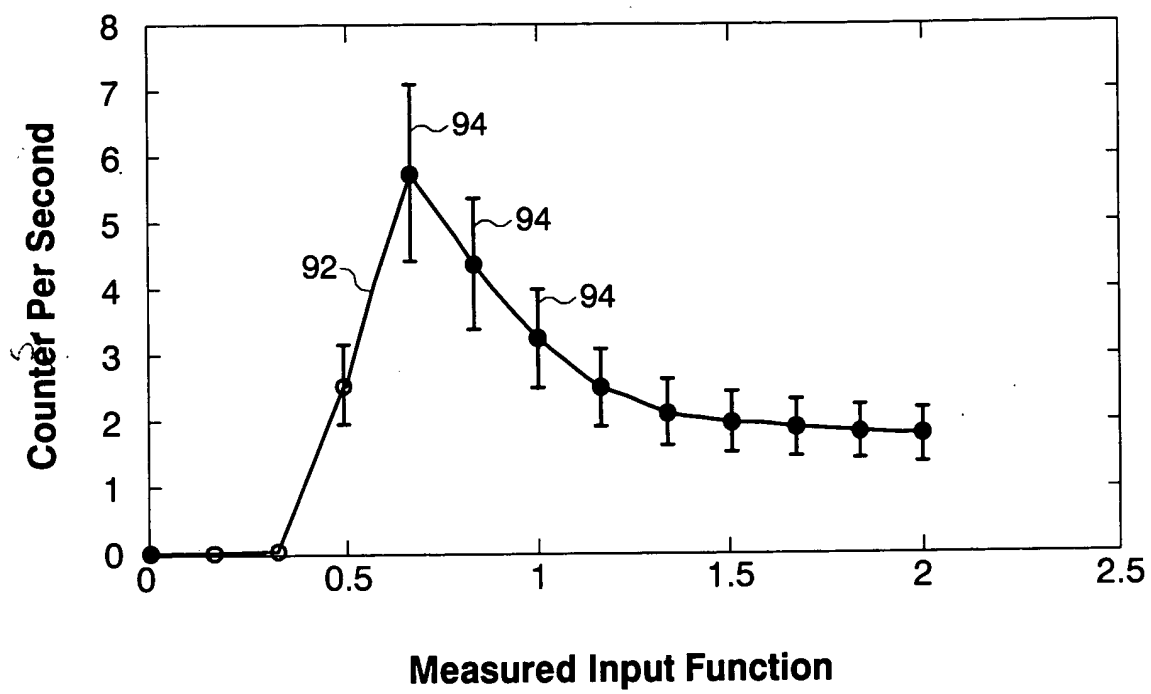


Figure 25

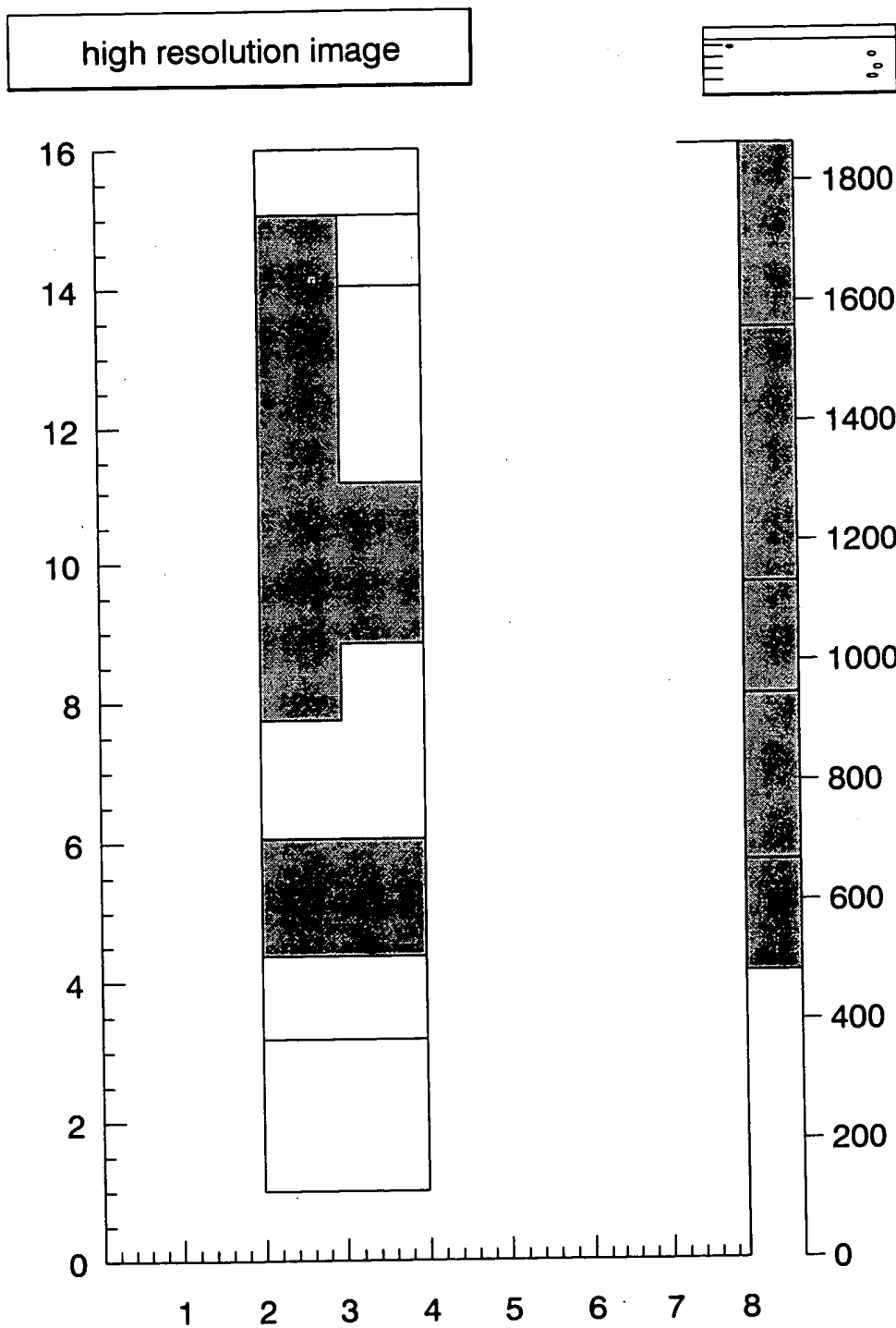


Figure 26

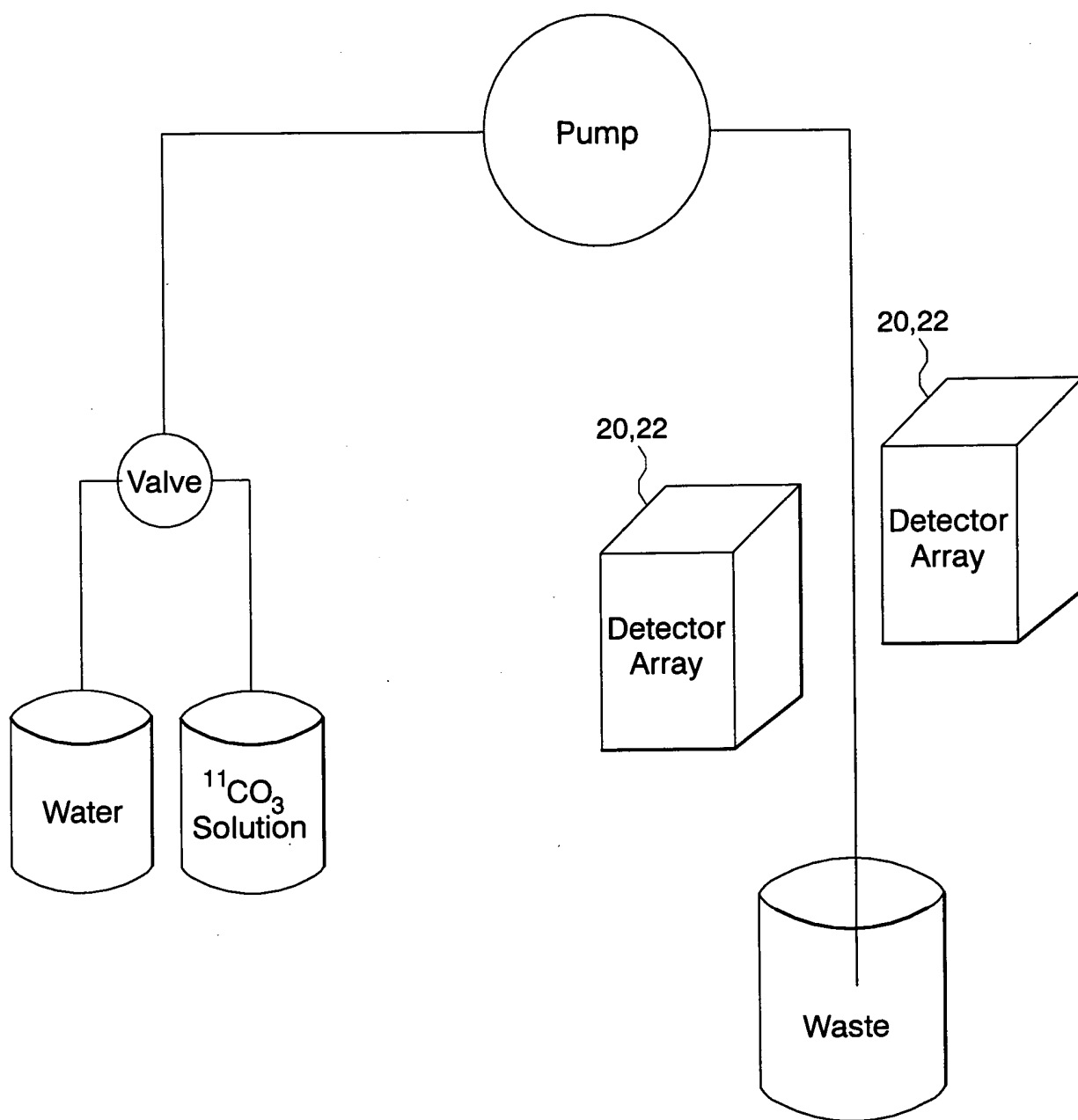


Figure 26a

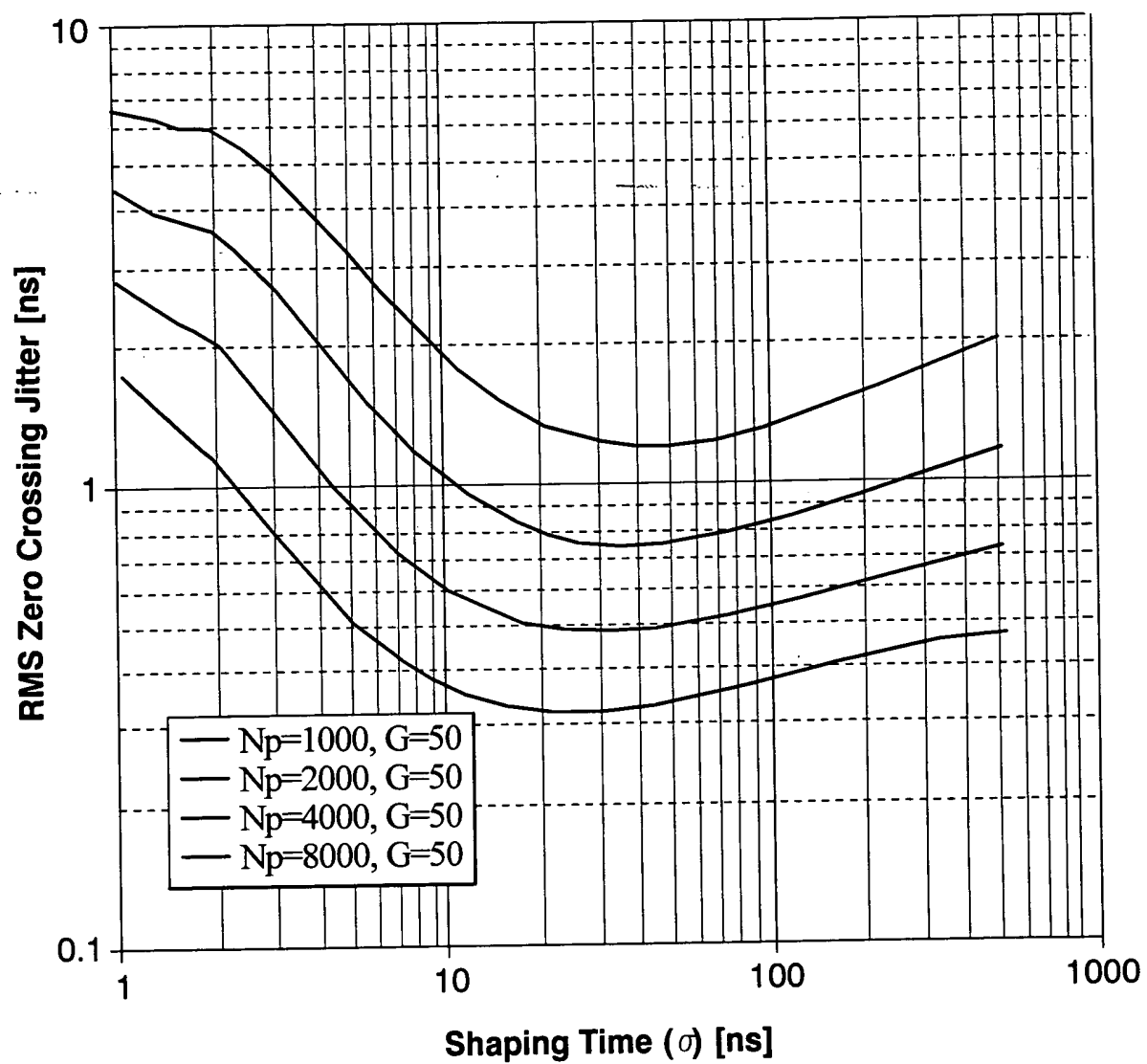


Figure 27

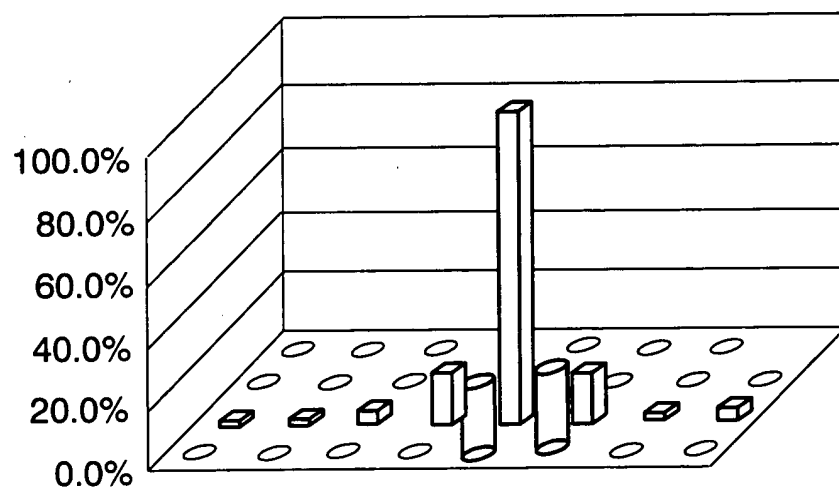


Figure 28